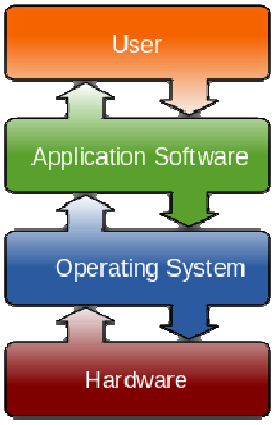
SCSX1027 HARDWARE PERIPHERALS AND INTERFACING

UNIT I – CPU AND MEMORY

CPU has 3 parts:



1. ALU

2. Control Unit – communicates to other parts of hardware, decide instructions and determines which is next to be executed.

3. Buses and Registers –

- It is a path for information entering and exiting the CPU.
- Registers are memory for processing informations.eg-program counter, instruction register
- Registers single storage location within the CPU

CPU ESSENTIALS

- Buses
- processor modes

The Microprocessor consists of several set of processor signals (or buses)

- Data Bus
- Address Bus
- Control Bus

The 3 buses allow the CPU to communicate with other elements in PC and control its operations.

Data Bus:

- Carries information from the CPU
- Number of wires in the bus represents the number of bits (or volume) that can be carried at any point of time
- Data lines labelled as (D0, D1……. Dn)

Address Bus:

- It is used for the CPU read and write data and it must be able to specify the location in system memory.
- Location defined by address bus.
- Number of bits in the address bus represents the number of physical location that the CPU can access

CONTROL BUS:

- Used to synchronize and coordinate the operations at the CPU with other devices
- The control signals are used in to
    - reading or writing functions
    - interrupt channels
    - CPU test and reset
    - DMA ctrl
    - CPU status
    - Parity checking
    - Chace operation
    - Power ctrl management

PROCESSOR MODES:

- Real mode
- Protected mode
- Virtual mode

The processor nodes controls how the processor sees and manages the system memory and tasks that use it.

REAL MODE (8088):

- original IBMPC could address IMB of system memory
- The processor had to support a mode compatible with original intel 8088 chip
- Processor is running in real mode. It has advantage of speed. Otherwise it can acess IMB memory and does has the advantage of full 32 bit processing of modern CPU.
- Real mode is used in DOS mode and standard DOS application.
- DOS is single tasking.

PROTECTED MODE (80286):

- IBM AT introduced a new processor mode is protected mode
- It is powerful than real mode
- Used in all moder multitasking OS
- Full access of system memory
- Multitasking
- Virtual memory
- Protection fault- if a program tries to use a memory address that is not allowed it is also called enhanced mode

VIRTUAL REAL MODE:

- If u want to run DOS program under window, there is problem to run DOS in windows.
- DOS program runs in real mode
- To solve this problem the virtual real mode is essential. It emulates real mode from within protected mode allowing DOS program to run
- Windows can create multiple virtual real mode machines and get its 1MB space

MODERN CPU CONCEPTS

1. CISC vs RISC (complex instruction set computing, reduced instruction set computing)
2. Circuit size and DIE size
3. Processor speed
4. Version and steps
5. Processor power management
6. Processor cooling
7. System clocks
8. Processor packages
9. The P-Rating (PR system)

CISC VS RISC:

CISC

- Traditional CPU are based on CISC architecture
- This approach allows any number of instructions to be used in the CPU
- CPU must provide all the internal circuitry needed to process each instuctions
- Each new instructions requires many new transistors for processing CISC CPU are typically found in general purpose desktop.

RISC

- Uses limited number of very powerful instructions.
- This CPU requires fewer transistors in the CPU for processing.
- This results in faster CPU performance with lower power consumption.

CIRCUIT SIZE AND DIE SIZE:

CIRCUIT SIZE

- The circuit size relates to the level of miniaturization (process of making small) a process.
- To make more powerful processor more transistors are needed.

- Technology advancements in IC fabrication allow circuit size to shrink. The fabrication technology shrunk as low as 0.008 microns.

DIE SIZE

- The die size processor refers to the area of the chip and it is measured in square millimeter (mm^2).
- Small die size consumes less power.

PROCESS OR SPEED:

- Speed is related to design of the processor circuit.
- Speed is influenced by manufacturing factor such as die size and circuit size.
- Smaller chips can run faster because of shorter signal run and low power consumption.
- Processor are related to the speed during the testing and manufacturing process.

VERSION AND STEPS:

- The processor represents very complex design. The existing processor may have bugs.
- The older version bugs are fixed and the problems can be encountered in the newer version.
- Intel using the term stepping to indicate process or revision
- S-spec typically marked right on the processor.

PROCESSOR POWER AND MANAGEMENT:

- Processor consumes large amount of power
- To reduce power demands and improve performance in traditional.
- +5 volt has been given to the processors.
- The first step to reduce the operating voltage level is reduced to +0 to +3.3 volts.
- *SPLITRAIL*- new processor such as (P Max, II, III, IV) reduce the voltage levels using dual voltage. External (i/o voltage) is +3.3 volts and internal (core voltage)(+2.5 to +2.9v) latest processor (+1.80 to +2.4) volts.

PROCESSOR COOLING:

- Processor have a specified safe temperature range that represents the limit for normal operation.
- If the processor overheats, serious system problem will cause in the form at reboots, lockups, crashes, memory error, disk problem, application error.
- Processor are cooled by active heat skins which are composed of fast fan mounted to a large metal heat sink
- Heat sink pulls heat away from the processor and fan in turns cools the heat sink.

SYSTEM CLOCKS:

- Every modern PC uses multiple system clocks. Each clock runs at a specific frequency normally measured in mhz.
- *CYCLE*- A clock tick is the smallest unit in which the processing takes place.
- Original PC has a united system clock – A single clock drove the processor, memory, I/O bus.
- System clock is referred to the speed of memory bus running on the motor board.
- System performance is tied to the speed of system clock.

PROCESSOR PACKAGES:

- Rare chips are used directly, they are very fragile and sensitive.
- To protect the die or chip it is placed in a package and helps to dissipate heat.
- The standardized package normally takes in the form at slotted or socket device. Each sockets have different pins and voltage levels. Eg- socket 423 for p IV

  SLOT- Slot 1, slot 2, slot A

  SOCKET- socket 370, socket A
- *Overdrive*- processor technology became popular by replacing existing CPU with a pin compatible replacement processors that are operated at high internal clock speeds to enhance the system performance.

THE P-RATING:

- CPU can be equated to the Intel Pentium. Rating includes '+' or'++' suffix (PR 75++)
- It means CPU is delivering better performance than the corresponding Intel part.

ARCHITECTURAL PERFORMANCE

FEATURES

1. Super scalar architecture
2. Pipe lining
3. Super pipelining
4. Speculative execution and branch prediction
5. Dynamic execution
6. Register renaming and write buffer
7. Multiprocessing
8. Multimedia extensions

Super scalar architecture

- Program instructions are processed through circuits called execution units or execution engine
- Superscalar architecture refers to the use of multiple execution to allow the CPU to process more than one instructions simultaneously with every clock cycle
- By combining pipelining with multiple execution engines the super scalar architecture CPU are making extremely efficient use at every clock cycle.

Pipelining

- Instruction fetch
- Instruction decode
- Execute
- Memory access
- Register write back

- CPU process instructions and generate results through a complex series of transitions switches inside a CPU die
- Every CPU processed one instruction at a time and instruction is fetched and processed completely. It requires several clock cycles.
- Pipelining technique is also called as instruction pipelining as it allows a new instruction to start while a current instruction is still processed.

Super pipelining

- Instructions are processed in a pipeline with each step in the processing. Pipeline perform certain amount of instruction.
- By making pipeline larger (with more stages) each stage perform less work and the processor can be scaled on higher clock frequency.

Speculative execution and branch predictions

- It is a optimization technique which performs some task that is not actually needed. So before work we want to know whether it is required so we can avoid time delay.
- Branches represents a problem for pipelining, because we can't assure that instructions will go in a linear sequence
- Advance processor combines with branch prediction where the processor can actually predict which way the branch will go based on the past history.
- *Branch target buffer*- Branch prediction improves the handling of branches by making use at small cache called branch target buffer

Dynamic (out-of-order) execution

- The dynamic execution technique allows the processor to evaluate the programs flow and choose the best order in which to process instruction.
- The results of the execution reassembled in the current order to ensure the program run correctly.
- eg-instruction 2 can be executed before instruction 1executed.

Register renaming and write buffer

- Renaming is a technique used to support multiple execution paths without conflicts between different execution units trying to use same registers.
- *Write buffer*- It is used to hold the results of instruction execution until they can be returned back to register or memory locations.

Multiprocessing

- Divided in to Asymmetric and symmetric.
- Running a system with more than one processor, double system performance.
- *Quadruple performance*- using four processor instead of one to empty multiprocessing effectively.

- *Threaded*- application designed for multiprocessing called thread. They are broken in to small routines that can be run in more than one processor simultaneously.
- *Asymmetric* – It designates some processor to perform system tasks only and other to run application applying poor performance.
- *Symmetric* –Allow either system or user tasks to run on any processor. It is more flexible and gives better performance.

Multimedia extensions –MMX

- In 1996 Intel introduced MMX extensions with powerful 57 new instructions.
- It process multiple data elements in a panel using a technique called SIMD (single instruction multiple data)
- SIMD allow process to be performed large amount of data simultaneously and reduce overall processing and it handles large amount of video and audio multimedia information
- *3D-Now* (1988) - AMD introduce 21 new instructions on 3D related features that significantly enhance the processing at 3D graphics images.
- *SSE & SSE* II (1999) – Intel updated its multimedia extensions by introducing SSE (Streaming SIMD extension) for p II. SSE builds on MMX by adding 70 new instructions to enhance advanced imaging, 3D graphics.

THE INTEL CPU

8086/8088 (1978-1979)

- 29,000 transistors
- 16 bit microprocessor
- 16 bits data bits are available
- 24 registers are available in 8086/8088.
- 20 address lines able to access 1mb of system memory
- 8086 available in4 clocks speeds, 5mhz, 6mhz, 8mhz, 10mhz.
- It process 0.33,0.66,0.75MIPs (Million of instruction per second)

80186

- 16 bit processor
- Offers additional features

- Internal clock generator
- System controller
- Interrupt controller
- Direct memory access controller
- Timer/counter circuitry

- Clock speeds 8mhz,10mhz,12.5mhz
- 24 register & 20 address lines

80286 (1982)

- It have 24 registers & 134,000 transistor CPU.
- Operate at 1.2m/Ps ,1.5m/Ps, 2.66m/Ps
- Direct access at 16mb of RAM, handle up to 1GB of virtual memory
- Draw back:It switches from real mode to protected mode and it cannot switch back to real mode of warm reboot of system.

80386 (1985-1990)

- 27,500 transistor
- 32 register with full 32 bit data bus.
- 32 bit address bus allows 4GB RAM & handle 64TB virtual memory.
- 1st Intel CPU enhances processing through Instruction Pipelining.
- *Virtual real mode* – it enables CPU to run several real mode session simultaneously under OS.

80486 (1989-1994)

- It has 1.2 million transistors.
- 29 registers
- 32 bit data bus.
- 32 bit address bus access 4GB at RAM & 64TB of virtual memory.
- Uses pipeline to improve instruction execution.
- 8KB of cache memory.
- *Cache* – saves memory access by predicting the next instruction that will be needed by CPU & loading in to the cache memory before CPU actually needs.

Pentium (1993-1998)

- 3.21 Million transistor Pentium
- 32 bit address can access 4GB of RAM can access 6TB of virtual memory.
- Two 8KB cache (total 16KB) one for instruction and other for data.
- *Dual pipeline*- works on more than one instruction per clock.
- 512 KB cache is the maximum.

Pentium (1995-1999)

- The processor range from 150mhz to 200mhz can handle multiprocessing in system up to 4 CPU
- Two 8KB L_1 caches, one for data and one for instructions.
- 1MB L_2 cache maximizes processor performance.

Pentium MMX (1997-1999)

- Added 57new MMX instructions in existing Pentium architecture.
- 10-20% faster than classic perform processor at same clock speed.
- 16KB cache double the code and data.
- Super scalar Architecture is introduced.

Pentium II (1997-current)

- Use with 32 bit OS and software.
- P II includes 57 new instructions handle MMX application.
- Dynamic execution Uses multiple branch prediction to predict the flow of program through several branches.
- 32KB – L_1 cache, 16KB for data, 16KB for instruction.
- Supports 64GB at physical RAM allows dual processors.
- Allow 512KB OF L2 cache.

Pentium II overdrive (1998-current)

- It is produced by Upgrading Pentium pro (socket8) processors.
- Upgraded for increase the performance and speed.

Pentium II/III CELERON (1988- current)

- 0.18 micron processor using Socket 376.It has 32KB L_1 cache.
- Celeron processor and integrated L_2 cache.
- FC-PGA package (flip chip – pin grid array) is socket 370. Eliminate (SEPP or slot 1) for cost reduction.
- Celeron with 266mhz to 433mhz are available in single edge processor package (SEPP)-Slot 1.Eliminate (SEPP or slot 1) for cost reduction.
- Celeron with 300mhz and up are available in plastic pin grid array (PPGA) and FC-PGA style package.

Pentium III (1999-current)

- Introduction of higher speeds and processor to utilize 13mhz front side bus (FSB)
- Intel streaming SIMB extensions (SSE) technology is used.
- It has 32KB L_1 cache & 512KB L_2 cache.
- It uses up to4GB RAM, the processor speeds are 450mhz to 600mhz
- Intel introduced processor serial number (PSN).
- This number allows individual processor to be identified remotely over a network.

Pentium II/III XEON (1999-current)

- It is a high performance model of Pentium II/III family.
- L_2 cache speed equal to core processor speed.
- Xenon processor is available with L_2 cache amounts 512KB,1MB, 2MB.
- L_2 cache is placed in die so it is used as slot2.

Pentium IV (2000-current)

- It is a 42 million transistor and produced in a socket style package currently known as PGA.
- It has 423 pin socket olga on interposer (OOL) package.
- Future Pentium 4 will be produced in a 428 pin package.

Features

- Additional SIMD instruction.
- Hyper pipelining and rapid execution
- Advance level 2 cache

- Advance dynamic execution
- 400mhz system bus

Additional SIMD Instructions

- The existing SSE Streaming SIMP Extension have been augumented with i44 new instructions or improved SIMD extensions(SSE_2)
- SSE_2 allows P4 to utilize 128 bits of data at once and it improves data handling.
- New instructions are used to improve multimedia performance, Speech Recongnization, 3D operations.

Hyper pipelining & rapid execution

- It doubles the pipeline depth
- Rapid execution helps to run two arithmetic and logical unit running at two times the frequency of the core processor.
- So simple (Add, Sub) requires ½ clock cycle.

Advanced level 2 cache

- L_2 cache design at p4 is 32 byte interface that transfer data on each core clock cycle.
- The cache is located on die and operates the core speed of the process.

Advance dynamic execution

- Expanded speculative execution.
- Allows P4 to view 126 instructions in the pipeline.
- Provides enhanced branch prediction.
- Reduces the branch busses

400mhz system bus

- Quad pumping that allows for a effective data transfer make at 400mhz on a 100mhz system bus.
- This can deliver 32GB of data per second in and out of the processor.

CPU OVERCLOCKING

- Overclocking means of maximizing the performance of an existing CPU.
- Overclocking is basically the practice of the configuring a PC to operate a CPU at a higher clock speed.

Overclocking requirements- 4 critical elements

- CPU
- motherboard
- system RAM
- CPU cooling

CPU issues

- Intel especially Celerons seems to be most successful at overclocking.
- AMD & VIA cyrix CPU are often running very close to their rated limits already in effort to compete with intel.
- But not all intel CPUs are suitable.

Mother issues

- If CPU is perfect for overclocking and the motherboard may not be.
- Signal reflection and other electrical limitation with in bus signals can cause the system crash or hang.
- Overclocked CPUs are very sensitive.
- Unstable signals from the bus will crash and the motherboard can't deliver clean signals.
- Most classic motherboard supports the bus speed up to 66 or 100mhz.

RAM issues

- System RAM can also be a problem with bus speeds that exceeds 66mhz.
- So we require high end EDO RAM or SDRAM.
- Extended data o/p RAM.
- Synchronous dynamic RAM.
- EDO- works with 66mhz motherboards.

- Low end SDRAM- Best with 75mhz &83mhz
- DDR-SD RAM- Double data rate SDRAM and RDRAM – Rambus dynamic RAM support faster speeds.

Cooling issues

- Problem with CPU overclocking is insufficient cooling.
- More cycles in a given period that more current is required and more heat is generated.
- Overclock a CPU can easily overheat and crash.
- You should never attempt to overclock a CPU without making accommodation at better cooling.
- Liquid cooling cilling system ,latest piezo electric cooling.

Overclocking the system

- Turn of the computer
- Check the marking on the top and bottom of your cpu and reinstall the cpu
- Check the current clock and multiplier jumper setting on your motherboards.on jumper less motherboards you can usually find information in cmos setup.
- Inspect the cooling unit on your cpu and upgrade the cooling unit is necessary
- Change the jumper setting for clock speed on jumper less motherboards you can usually alter these setting in cmos setup
- Double check the new setting are configured as expected.
- Start the computer and allow it to boot on cmos setup
- Does it boot or reach the cmos setup, if no.
- Turn off and change the cpu voltage jumper to a slightly higher voltage
- If you still cant boot or reach the cmos setup return the voltage setting to its original vaue.you can overclock at this desired speed.return the clock speed and multiplier setting to original & quit.
- You may need to adjust RAM or bus timing to accomodate the changes to your processor setting.
- Does the system boat to afull working operating system?.if nocheck the cooling system & cmos if yes next step
- Check any crashes in system operation .if the system proves unstable you cannot overclock at this level .return the clock speed and multiplier the original value and quit

- Every thing works well change the bus speed
- The internal clock of a cpu runs at a different speed than the external clock (fsb speed)
- The external clock is the speed at which the cache and main memory run and usually divided down to yield suitable clock signal for the agp bus & pci bus and other bus In the system.
- To change the bus speed select external bcy frequency or fsb frequency.
- There are jumper to change
- For jumper less mother board use cmos setup

Change the multiplier

- The cpu internal clock is controlled by the clock multiplier in each cpu.
- Which is programmed via cpu pins .intern cpu support the following multiplier *2 ,*2.5,*3, p ii /ii uses *3 to *7 and more
- Change the multiplier setting .there are several jumper used to change these setting .(clock multiplier or cpu ,bus frequency)

Change the supply voltage

- When booting the cpu supply voltage (from 3.3vstd to 3.45 vre(voltage regulation extended)) may be necessary to make the cpu at a higher bus speed.

Higher bus speeds

- Pentium class mother boards handle upto 66mhz, Pentium mmx operate at 75mhz to 83 mhz.

PCIbus issues

- The pci bus is taken from the clock speed at 60 or66 mhz
- The pcibus speedis 30 to 35 mhz
- 75 or 8 mhz clock speed motherboards the pci bus at 37.5 or 41.6 mhz respectively
- The faster speed can lead problem with some pci devices.

EIDE bus issues

- Enhanced integrated device electronics
- The speed of an eide is not only determined by dma modes but it is highly dependent on pci clock.
- The eide interface will be faster when you are running at higher pci bus speed

ISA bus issues

- Isa bus speeds is divided directly from the pci bus.
- If pci was running faster then isa also runs faster.
- The fsb is increased to 100mhz & 13mhz.
- The chip sets have beeb developed to include dividerthat maintain pci bus speeds. Pci-33mhz.agp-66mhz

AGP bus issues

- The agp bus is designed to operate 66 mhz usually as the traction of system bus speed.
- At 100mhz or 133mhz system bus the agp bus speed at 2/3 or ½ respectively.
- At 60 mhz the agp bus speed is 1/1.
- Overclocking the system bus can also overclock the agp bus.

Overclocking the INTEL processor

- Inter Pentium end Pentium mmx processor have traditionally.some of the easiest cpu to overclock.

Overclocking INTEL Celeron

- The Celeron Pentium ii core lower price and high production quality combinely attract the user looking for performance gains through overclocking.
- Intel sought to limit the Celeron use in overclovking with a locked multiplier and locked bus speed of 66 mhz.
- With the implementation of lockrd multiplier half of the processor speed capability has been eliminated for overclocking.
- Eg 600mhz Celeron processor where the multipliers locked at 6x.we can adjust the fsb in the motherboards in 5mhz increments.
- 6*100mhz=600mhz(standard)
- 6*105mhz=630mhz(overclocked)
- Modern motherboard offer 66mhz to 170mhz
- The ability to successfully overclock a Celeron cpu may also depend on the availability higher voltages .
- It some time takes a little more voltage to reach a faster signal speed.
- Eg celerofoo 92 mhz*105=966 mhz-1.8v (overclock) 83mhz *10.5=875 mhz (1.7v) std

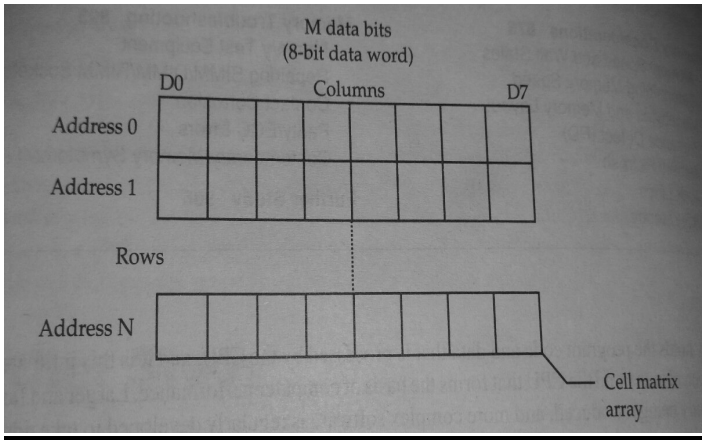
Overclocking intel Pentium ii / iii

- Pentium ii processors are manufactured using a 0.35 micro processor were available in 233mhz to 300mhz using a66mhz fsb.
- Intel then introduce 0.25 micro processor pii at the speed of 333mhz to 450mhz
- 333mhz pii use 66mhz fsb 350mhz & up use 100mhz
- The first p iii processor was manufactured using 0.25 micron were available in 450mhz to 600mhz.
- P iii using 0.18 micro process available in speeds from 500 mhz & up
- 1988 intel has been locking the clock multiplier on its cpu
- We cannot change the multiplier when overclocking 350mhz,400mhz,450mhz p ii or p iii or p iv.
- For instance overclocking a 100mhz fsb to112mhz results in the pci bus being overclocked to 37mhz(33mhz) 2d agp bus overclock 774mhz(66mhz).
- Increasing the speed after fsb also increases the speed of pci & agp.

Essential memory concepts

1. Memory organization.
2. Memory signals

Memory organization



- All memory is basically array of individual storage elements organized in to rows & columns.

- Each row-address
- Each column-data bits
- In address (row) there may be 1 million ,2 million,4million address on a single memory chip.
- Databits(column) an older memory chip may have one column of bits,but recent chip may have two or four columns of bits.

Cell: the intersection of each column and rows is an individual memory bit known as cell.

Memory signals: the array of memory bits communicate with three set of signals Address lines ,data lines, control lines .

Address lines ; define which row of memory array will be active .the address is specified in binary numbers.the conversion is done inside memory chip and translates binary number in to a specific row signal.

Data line: carry data bits back and forth to the storage cells of the defined address

Ctrl lines: used to operate memory chip eg:read write

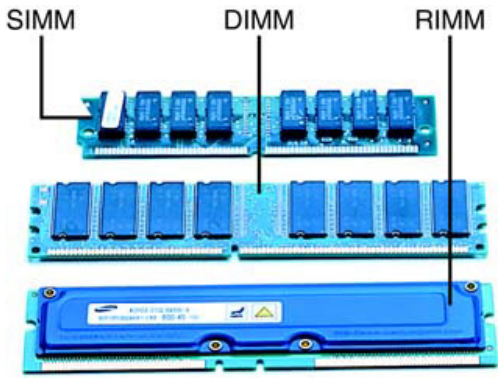
Signals example: a chip select (-cs) signal makes a memory chip active or inactive.ras (row address select) cas (column address select) to refresh operation.

Active or inactive: if the memory chip share common address for data the (-cs) disconnect from the circuit.

Memory package and structures:

Memory package- the memory package is mounted in a package just line any other chip. The complete memory package can be soldered or motherboard or attached to plug in structures such as SIMM,DIMM,RIMM

Memory modules:



SIMM- single inline memory module (1980-1990)

- Divided in to 32pin single sided and 72 pin double sided
- 32pin-(256 kb or 1MB) and 72 pin-32MB RAM
- 32 data bit data bus.

DIMM-Dual inline memory:

- 64 bit data bus width.
- Dimm support 64mb ,128mb,256 mb rom.

Dimm are placed on sockets in the mother board

72 pin DIMM type-FPM (first page mode),EDO Ram,

100 pin – SDRAM

172 pin- MICRODIMM DDRSDRAM

200 pin-DDR2 SDRAM

204 pin –DDR3 SDRAM

240 pin-DDR3 SDRAM

284pin-DDR4 SDRAM

Voltage:

- A voltage levels used on memory modules keep decreasing to manage heat & increase performance.
- Classical computer – std +5 volts
- Modern pc -3.3 volts & 2.5 volts
- Dimm - +5v & +3.3 volts

Registers and buffers:

- Registers and buffer improve memory operation by redriving signals in the memory crips.
- They can be external to the memory module or on the module.
- Buffering is used to redrive the signals in fpm,edo ram.
- Buffer – temporarily store data while it being moved from one place to another.

- Register is similar to buffer but the data is clocked for in and out of the register.

Composite and non composite:

- Used in apple computers.
- Explain the difference between modules of the same capacity that used at different no of chips.
- Module with the latest technology and fewer chips referred as non composite
- Module with earlier technology and additional chips called composite.

Rimm: rambus inline memory module (1990)

Drdram-direct rambus dynamic ram

Rdram-rambus dynamic ram used rim (168 pin)

Works twice the actual clock rate.

- Identical to dim.
- 168 pin
- 184 pin latest
- Rdram transfer 16 bit chunks along dedicate mrng.
- It also increased long heak sink manage rd ram chips.
- Chunks-fragment of information used in multi media formats

.**Five packages:**

Dip (dual inline package)

Sip (single inline package)

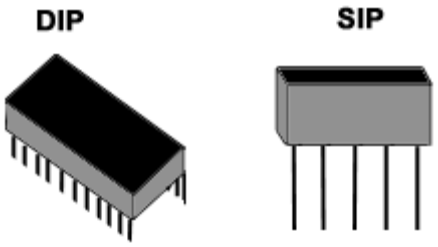
Soj(small outline j lead)

Tsop(thin small outline package)

Csp(chip scale package)

Dip:

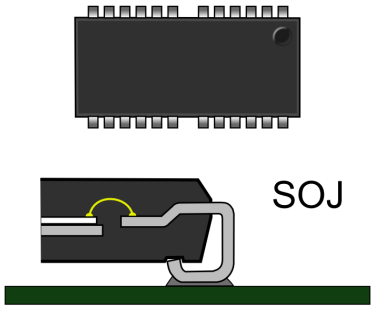
- Classical chip package used through hoce mounting (surface mount technology)
- Dip packages compatibility with socket allow chips to inserted or removed .
- Long pin if u remove or inserted incorrectly the pin will bend or break.
- Dual now of connecting pin.



Sip:

- Single row of connection pins.
- Use in late model 286 and 386 systems.
- Rarely used it is trouble to find replacements.

Soj:

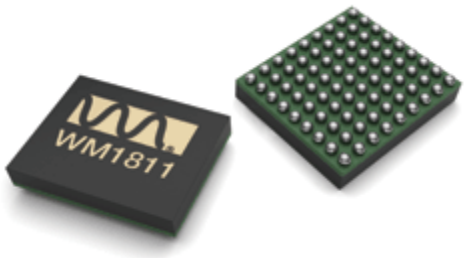


- Surface mount circuits .
- Like dip but pins are bent around just under the package in the form of eg: bios rom.

Tsop:

- Like soj ,Tsop is surface mount package style.
- Soj pin bending under the package.
- Tsop the pin extend away.
- Find in note books.

Csp (chip scale package):



- Does not use pin to connect.
- Packages uses a series of surface mount contacts pads under side of chip.

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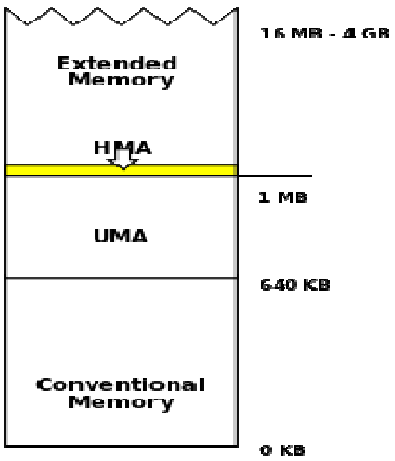
LOGICAL MEMORY ORGANIZATION

- Logical memory enables the user to use large amount of memory to store data.It is used how to organize the physical memory ram & cache.It enables os to arrange logical manner by assigning logical address._Logical address is a memory location accessed by the application pgm.During execution of the pgm the system maps the logical address of the physical_Storage address.Physical address space divided in to page frames.



Conventional memory:

- It is traditional 640 kb which was used by dos & application.
- The original pc used microphones that could address 1mb of memory.
- Real mode or base memory.
- Out of 1mb portion of memory that set basic functions bios code & drivers.

Extended memory(XMS):

- Protected mode.
- Memory area is extended to above 1mb.
- Xms available in 80286 processor.
- 286 xms up to 16 mb.
- 386 xms up to 4gb.
- Dos does not use Xms
- Windows& os use Xms
- We can view these details mem commnd in the cmd prompt.

Dos extender:

- The dos extender converted protected mode address in to the real mode addressing.
- To prevent conflicts in the extended memory.
- The memory manager s/w can take use at 3 majors standard.
- Extended memory specification(xms).
- Virtual ctrl program interface(vcpi)
- Dos protected mode interface (dpmi)

Expanded memory system(EMS);

- Another technique to overcome 640kb limit real mode.
- Ems card was developed that would plug in the expansion slots
- Ems hold extra 32mb of ram.
- Ems ability to map directly to the real mode support multitasking.
- Expanded memory is the memory available in expansion adapter card.

Upper memory area: (UMA)

- Memory lines lies between 640kb 21mb -1024kb.
- Dos only uses 640kb.
- The upper most 384 kb space for bios rom,video ramand peripherals,10 port expansion cards.
- Eg: video memory area 704 to 736 kb.

High memory area:

- it is a ram area consisting of the first 64 kb of the extends memory beyond real mode area.
- The real mode operation can access roughly 64 kb above the 1mb limit.
- High dos memory 64kb not contiguous with the normal 640 kb dos memory range.

MEMORY TYPES

- The cpu must take program instruction & exchange data directly with memory.
- BEDO(burst extended data output ram)
- CDRAM (cache ram)
- DDR-SDRAM
- DRAM(dynamic ram)
- EDORAM
- EDRAM(ENHANCED DYNAMIC)
- FPM(Fast Pagemode Ram)
- SDRAM (synchronous dynamic ram)
- SGRAM(synchronous graphics)
- SRAM(static Ram)
- VRAM(video ram)
- WRAM (window Ram)
- RDRAM(Rambus dram)

RDRAM:

- Used in 133mhz bus speed mother boards.
- Operating at 100mhz to 1000mhz.
- Can transfer data on beta edges of the block.
- Uses pipeline memory architecture.

WRAM:

- Samsung electronics introduces a new video specific memory device.
- Wram – user multiple bit array connected with as internal bus & high speed registers.
- That can transfer continuosly 640 mb data.
- 50% faster than video ram.
- Cheaper than vram and sdram.

SGRAM –synchronous graphics:

- Video specific extension of sdram.
- Includes graphics optimized read/ write features.
- All data to be modified in to blocks that readers reads and writes.
- Increase the performance of graphics controller.

CDRAM:

- Cache dynamic mistubushi incorporates cache & dram.
- Eliminates the need of l2 or external cache.
- Benefit adding of cache whenever ram is added on the system.
- 15-20% faster than ed ram.

EDRAM:

- Enhanced ramtron international & unified measures introduced edram.
- Like page mode memory.
- It reads requests data that presenting edram cache known as cache hit.
- Read request data that is not in cache called cache miss.
- Faster than dram.

DDR SDRAM:

- It allow to transfer data on both rising and falling edge of the system clock.
- So speed of memory access increases.
- It can be effectively double the speed atleast 200mhz – 266 mhz.

DRAM:

- A single transistor and capacitor is neede to hold a bit.
- Dram contents must be refreshed every milliseconds.
- The content of each location bit will decay.
- In lowered video boards continue to use dram chips to supply video memory.
- Ras-row address select
- Cas-column address select
- To do read / write operation
- Use 66 mhz bus speed access 60ns or 70ns.

EDORAM:

- Storage cells- (rows & columns)
- Row- word lines
- Column-bit lines
- It take 5 clock cycles to read the first word & sub – sequent words are ready in every 2 clock cycles
- 5-2-2-2
- Used in Pentium system above100 mhz access the memory 50 or 60 or 70 nos

BEDO:

- Powerful than edo read data In the burst mode.
- Means that after valid address has been provided.
- 5-1-1-1-1
- 5 times faster than edo
- Burst is temporary high speed of data transmission at medium through put.

SDRAM:

- The speed of memory is synchronized with the speed of cpu.
- Operating speed is up to 100mhz – 133 mhz.
- 5-1-1-1 pattern transfer data.
- On chip burst counter is used to read data sequentially.
- Memory controller is used to given location and size of block.
- Pipeline burst – allow the second instruction to begin before the current instruction completed.

S-ram:

- Developed by monolithic system.
- Sram is built with 4 or 6 transistor to hold single bit.
- Faster than dynamic ram.
- Speed at s ram has earned by pc L2 or external cache.

VRAM:

- Dram is used in traditional video ram.
- For fast video information.
- Vram is introduced by Samsung
- Vram achieve speed by dual data bus.
- Dual data bus allows data to read from vram at a same time new instruction is written to it.

FPMDRAM:

- Fast page mode over come this delay by allowing the cpu to access multiple pieces of data on the same page.
- Without relocate the page everytime
- Fpm reduce power consumption.
- The minimum cycle is 5 ns
- 6-3-3-3.

Memory techniques

- There are four popular architecture,
    - Paged memory.
    - Inter leaved memory.
    - Memory cache.
    - Shadow memory

Page memory:

- It divides system ram in to small groups or pages form 512bytes to several rb.
- The memory management of the mother board allows subsequent memory access on the same page with zero wait states.
- When new page found one or more wait states may be added.

Interleaved memory:

- It combines of two banks of memory in to one'
- Better than paged memory.
- 1^{st} partition is even, 2^{nd} is odd.
- So memory contents are alternated between two areas.
- This allows a memory access in second portion begin before the first portion has finished.
- Improve memory performance.

Memory cache:

- Cache is a small amount (8 kb to 1 mb) of very fast memory that frames the interface between cpu & dram.
- Keep cpu with zero wait states .
- A cache controller chip on the mother board keep track frequently the predicted memory location which the contents available.

Cache hit:

- When cpu needs memory it checks the cache first if data is available is called cache hit.
- Not available called cache miss.
- Ramacts as index , recording the various location of data in cache –(l1 internal , l2 internal).

Shadow memory:

- Rom contents are loaded into area of fast ram during system initialization.
- Then computer maps the fast ram in memory location used by rom devices.
- Rom routines are accessed during the run time.
- Rom devices are slow with access time of exceeding several 1000ns.
- Rom access requires a large number of wait states which slow down system performance.
- Information is taken from the shadowed ram is faster instead of the actual rom chip.

Memory considerations:

- Memory speed & wait states.
- Determining memory speed.
- Mega bytes & memory layout.
- Presence detect (pd)
- Memory refresh.
- Clock lines
- Cas latency
- Bursting & pipelining

- Memory has importance to store bits for the micro processor.
- Speed should be measured in term of access time.
- Pull a piece of data from memory and get in on to memory after processed.
- Measured in nano seconds.
- Beginning of using sdram speed was measured in term cycle time.
- Cycle time to sdram 12,10 8ns.

Wait state:

- Command to pause the cpu for one clock cycle in order to give memory additional time to operate.

Determining memory speed:

- During trouble shooting or the replacement parts.
- It is necessary to check memory module for memory speed.

- Marking specifiers the memory speed.
- Eg : sdram -12 for 12ns cycle time.

Mega bytes & memory layout:

- Megabyte is 1 million of byte
- 1byte-8 bits (0's & 1's)
- Denoted by mb
- Used to measure the memory in pc.

Presence detect:

- To know configuration of what memory is present & what timing to use to access memory.
- Modern memory devices is a series of physical signals known as presence detect lines.
- Presence Detect specifies two operating characteristics

  1, size(device layout)

  2,speed

Memory refresh:

- Electric signals are used in dram.
- Dram storage cell must be refreshed periodically every few millisecond.
- Without refresh dram will be lost.
- Refresh requires that storage can be read & rewritten to the memory array.

Clock lines:

- Sdram memory requires either 2 or 4 clock signal line between the system clock & memory module.
- Memory modules with 2 clock lines – two clock sd ram (older)
- Memory with 4 clock line.
- Four clock sdram (newer).
- Clock lines- used to decrease the sgl load & enables quick data interface.

Cas latency: (cas)

- Measure latency of memory chip.

- How long time takes to a initial read comment is sent to memory the first piece of result data is output.
- Measured by clock cycle.
- Cl2 – two clock delay
- Cl3- three clock delay

Bursting:

- Data is send faster than normal, tradionally only one piece of data is handled in memory access cycle. It is a performance improvement
- Process retrieve block of from consecutive memory.
- Used when reading & writing data.

Pipelining:

- Task is divided in to a series of stages .
- Each step some work should be done.
- System performance.

Un buffered:

- Un buffered memory module contains only memory devices.
- Data passed between memory chips is not boosted by buffer on the module itself.
- Buffers & registers to the memory module the electrical signals entering & leaving the memory module & strengthen the module'
- The process of retrieving memory signal is called buffering.
- (data one place to another temporarily is stored in buffer , it is physical memory storage)