SEC1205 - ELECTRONIC CIRCUITS - I

UNIT 3 SMALL SIGNAL ANALYSIS OF FET AND MOSFET AMPLIFIERS

Biasing of FET Amplifiers- Types- Small Signal Model of FET- Small Signal Analysis of CS-CD-CG FET Calculation of Input Impedance-output impedance-voltage gain using small signal model-MOSFET Biasing-Types-Small Signal Model of MOSFET-Small Signal Analysis of CS-CD-CG MOSFET- Calculation Input Impedance-output impedance - voltage gain using small signal model

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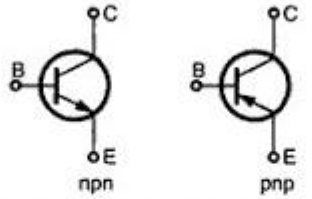
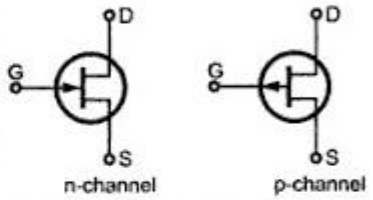
3.1 Comparison of BJT and JFET

Table 1 shows the comparison of Bipolar Junction Transistor (BJT) and Junction Field Effect Transistor (JFET).

Table 1. Comparison of BJT and JFET

Sr. No.	Parameter	BJT	JFET
1	Control element	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2	Device type	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3	Types	npn and pnp	n-channel and p-channel.
4	Symbols		
5	Configurations	CE, CB, CC	CS, CG, CD
6	Input resistance	Less compare to JFET.	High compare to BJT.
7	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	Thermal stability	Less	More
10	Thermal runaway	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temeperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11	Relation between input and output	Linear	Non-linear
12	Ratio of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14	Gain bandwidth product	High	Low

3.2 Introduction to Biasing of FET Amplifiers

Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. However, the wide differences in maximum and minimum transfer characteristics make it necessary to keep drain current I_D stable at its quiescent value. In this chapter we see the different d.c. biasing techniques for FET amplifier. The general relationships that can be applied to the d.c. analysis of all FET amplifiers are :

$$I_G = 0\ A \quad \ldots (1)$$

$$I_D = I_S \quad \ldots (2)$$

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \quad \ldots (3)$$

3.3 Types of JFET Biasing Circuits

- Fixed Bias
- Voltage Divider Bias
- Self Bias

3.3.1 Fixed bias Circuit

Fig. 3.1 shows the fixed bias circuit for the n-channel JFET. This is the simplest biasing arrangement. To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.

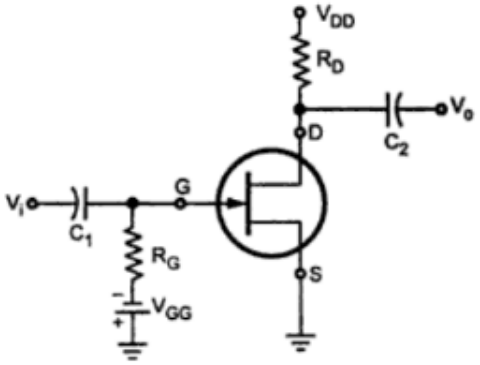


Figure 3.1 Fixed bias circuit for n-channel circuit

D.C. Analysis : For the d.c. analysis coupling capacitors are open circuits. The current through R_G is I_G which is zero. This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit as shown in the Fig. 3.2.

We know for d.c. analysis

$$I_G = 0\ A$$

and applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$\therefore\ V_{GS} = -V_{GG} \quad \ldots (4)$$

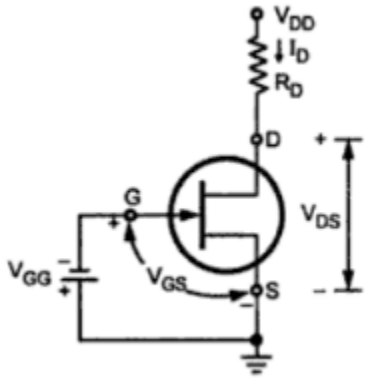


Fig. 3.2 Simplified Fixed Bias Circuit

Since V_{GG} is a fixed d.c. supply, the voltage V_{GS} is fixed in magnitude, and hence the name fixed bias circuit.

For fixed bias circuit the drain current I_D can be calculated using equation (3).

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

The drain to source voltage of output circuit can be determined by applying KVL.

$$+ V_{DS} + I_D R_D - V_{DD} = 0$$

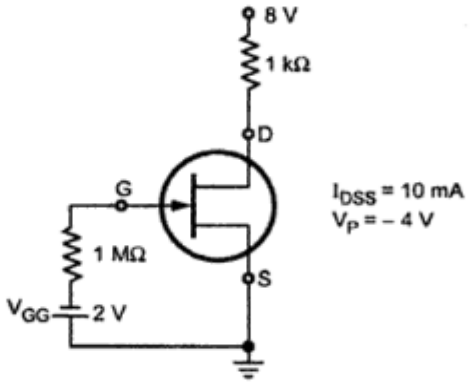
$$\therefore V_{DS} = V_{DD} - I_D R_D \quad \ldots (5)$$

The **Q point** of the JFET amplifier with fixed bias circuit is given by :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_{DQ} R_D$$

Example : *For the circuit shown in the Fig. Calculate :*
a) V_{GSQ}, b) I_{DQ},
c) V_{DSQ}, d) V_D



Solution :

a) $V_{GSQ} = -V_{GG} = -2\ V$

b) $I_{DQ} = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = 10\times10^{-3}\left(1-\frac{-2\ V}{-4\ V}\right)^2$

$= 10\times10^{-3}\ (1-05)^2 = 10\times10^{-3}\ (0.25) = 2.5\ mA$

c) $V_{DSQ} = V_{DD} - I_{DQ}R_D = 8\ V - 2.5\times10^{-3}\ (1\times10^3) = 5.5\ V$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = 5.5\ V$

3.3.2 Voltage Divider bias Circuit

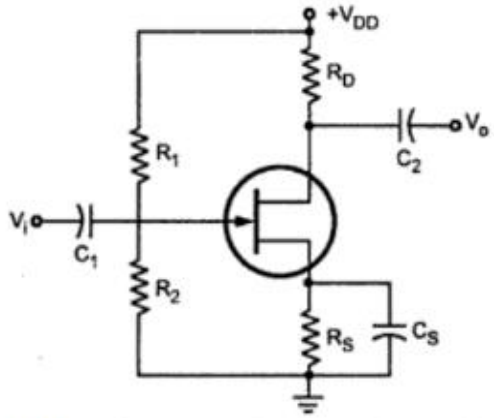


Fig. 3.3 **Voltage divider bias for n-channel JFET**

The Fig. 3.3 shows n-channel JFET with voltage divider bias. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased. The source voltage is,

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula :

$$V_G = \left(\frac{R_2}{R_1+R_2}\right)V_{DD} \qquad \because I_G = 0$$

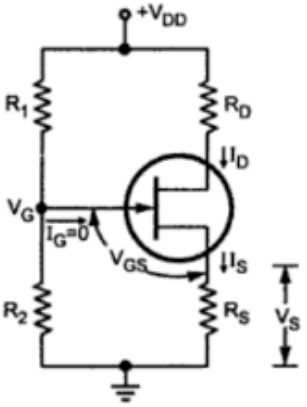


Fig. 3.4 **Simplified voltage divider circuit for dc analysis**

D.C. Analysis :

Applying KVL to the input circuit we get,

$V_G - V_{GS} - V_S = 0$

$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$

$= V_G - I_D R_S \qquad \because I_D = I_S$

$\therefore V_{GS} = V_G - I_D R_S \qquad \ldots (6)$

Applying KVL to the output circuit we get,

$V_{DS} + I_D R_D + V_S - V_{DD} = 0$

$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$

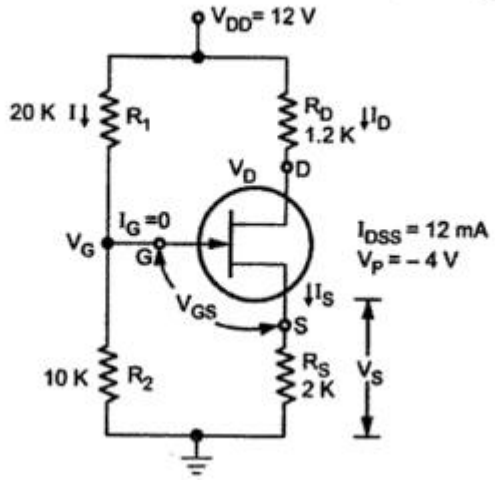
$= V_{DD} - I_D (R_D + R_S) \qquad \ldots (7)$

The Q point of a JFET amplifier using the voltage divider bias is given by :

$$I_{DQ} = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_D\,(R_D+R_S)$$

Example : *For circuit shown in Fig. Calculate* I_D , V_{GS} , V_G, V_{DS} *and* V_S.



Solution : We have,

$$V_{GS} = V_G - I_D\,R_S$$

where $$V_G = \frac{V_{DD}\,R_2}{R_1+R_2} = \frac{12\times 10K}{10K+20K} = 4\ V$$

$$\therefore V_{GS} = 4 - I_D\,R_S$$

We have, $$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} we get,

$$I_D = I_{DSS}\left(1-\frac{(4-I_D\,R_S)}{V_p}\right)^2 = 12\times 10^{-3}\left(1-\frac{(4-I_D\times 2\times 10^3)}{-4}\right)^2$$

$$= 12\times 10^{-3}\,(1-[(-1)+500\,I_D])^2 = 12\times 10^{-3}\,(2-500\,I_D)^2$$

$$= 12\times 10^{-3}(4-2000\,I_D+250000\,I_D^2)$$

$$I_D = (0.048-24\,I_D+3000\,I_D^2)$$

$$\therefore\ 3000\,I_D^2-25\,I_D+0.048 = 0$$

Solving quadratic equation using formula $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ we get,

$$= \frac{-(25) \pm \sqrt{(-25)^2 - 4(3000)(0.048)}}{2(3000)}$$

$$= \frac{25 \pm \sqrt{625 - 576}}{6000} = \frac{25 \pm \sqrt{49}}{6000} = \frac{25 \pm 7}{6000} = 5.33 \text{ mA or } 3 \text{ mA}$$

If we calculate value of V_{DS} taking $I_D = 5.33$ mA we get,

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$= 12 - 5.33 \times 10^{-3} (1.2K + 2K) = 12 - 17.07 = -5.07$$

Practically, the value of V_{DS} must be positive, hence $I_D = 5.33$ mA is invalid.

$$\therefore I_D = 3 \text{ mA},$$

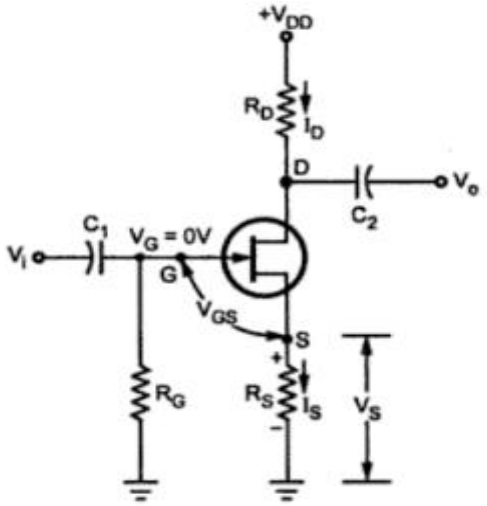
$$V_{DS} = 12 - 3 \times 10^{-3} (1.2 \times 10^3 + 2 \times 10^3) = 12 - 9.6 = 2.4 \text{ V}$$

$$\therefore V_{DS} = 2.4 \text{ V}$$

$$V_{GS} = 4 - I_D R_S = 4 - 3 \times 10^{-3} \times 2 \times 10^3 = 4 - 6 = -2 \text{ V}$$

$$V_S = I_D R_S = 3 \times 10^{-3} \times 2 \times 10^3 = 6 \text{ V}$$

3.3.3 Self bias Circuit



(a) n-channel

Note : $I_S = I_D$ in all JFETs

Fig. 3.5 **Self bias circuits for JFET**

Self bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. 3.5 . The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0V. R_G is necessary only to isolate an a.c. signal from ground in amplifier applications. The voltage drop across resistor, R_S makes gate source junction reverse biased.

For the n-channel FET in Fig. 3.5 , I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = - I_D R_S$$

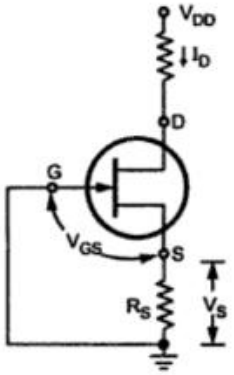


Fig. 3.6 **Simplified self bias circuit for dc analysis**

In the following D.C. analysis, the n-channel JFET shown in Fig. 3.5 is used to for illustration . For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig. 3.6.

We know, equation (3) gives relation between I_D and V_{GS}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2 \quad \ldots (8)$$

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D$$

$$= V_{DD} - I_D (R_S + R_D)$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D) \quad \ldots (9)$$

Example : *For the circuit shown in Fig. . Calculate* V_{GSQ} , I_{DQ} , V_{DS} , V_S *and* V_D

Solution : i) I_D : we have,

$$I_D = I_{DSS}\left(1+\frac{I_D R_S}{V_p}\right)^2$$

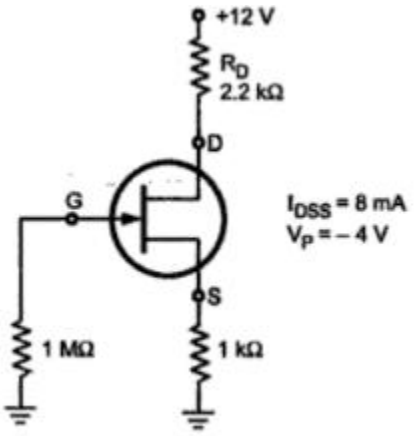
$$\therefore \quad I_D = 8\times10^{-3}\left(1+\frac{I_D\times1\times10^3}{-4}\right)^2$$

$$= 8\times10^{-3}\,(1-250\,I_D)^2$$

$$= 8\times10^{-3}\,(1-500\,I_D+62500\,I_D^2)$$

$$I_D = 8\times10^{-3}-4\,I_D+500\,I_D^2$$

$$\therefore \quad 500\,I_D^2-5\,I_D+8\times10^{-3} = 0$$



Solving quadratic equating using formula $\frac{-b\pm\sqrt{b^2-4ac}}{2a}$ we have,

$$= \frac{+5\pm\sqrt{(-5^2)-4(500)(8\times10^{-3})}}{2\times(500)}$$

$$= \frac{+5\pm\sqrt{25-16}}{1000} = \frac{+5\pm\sqrt{9}}{1000}$$

$$= \frac{+5\pm3}{1000} = 8 \text{ mA or } 2 \text{ mA}$$

I_{DQ} cannot have value 8 mA because maximum value of I_D, I_{DSS} is given as 8 mA at V_{GS} = 0 and hence I_{DQ} is taken as 2 mA.

ii) $V_{GS(Q)}$: we have,

$$V_{GSQ} = -I_D R_S = -2\times10^{-3}\times1\times10^{3}$$
$$= -2\ V$$

iii) V_{GS} : $V_S = I_D R_S = -2\times10^{3}\times1\times10^{3}$
$$= 2\ V$$

iv) V_{DS} : $V_{DS} = V_{DD} - I_D (R_D + R_S) = 12 - 2\times10^{-3}(2.2\times10^{3} + 1\times10^{3}) = 12 - 6.4$
$$= 5.6\ V$$

v) $V_D = V_{DS} + V_S = 5.6 + 2 = 7.6\ V$

3.4 Small Signal FET Models

The small-signal FET *model (valid both for JFET and MOSFET) is used to relate small changes in FET current and voltages about the quiescent operating point. The model is different at low and high-frequencies. Therefore we shall study the small-signal models separately as the low-frequency FET model and high-frequency model. In both these models, the FET will be considered in common source configuration.

3.4.1 Small Signal Low-Frequency FET Model

Figure 3.7 shows the small-signal low-frequency model of a field-effect transistor. In this model, the gate-to-source junction is represented by an open circuit and no current is drawn by the input terminal of the field-effect transistor. It is because of the fact, that the input resistance (*i.e.*, the resistance of gate-source junction) is very large. Its value at d.c. or zero frequency is typically 10^8 to $10^{10}\ \Omega$ for JFET's and 10^{10} to $10^{14}\ \Omega$ for MOSFET's. For all practical purposes, these values can be considered to be so large that the input of FET can be considered as an open circuit.

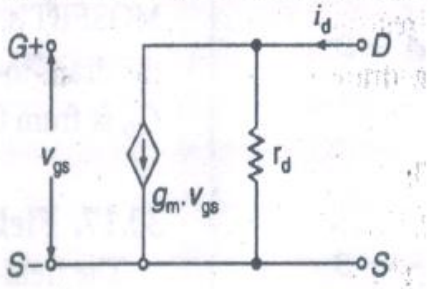


Fig. 3.7. Low-frequency FET model

It will be interesting to know that although the gate-source junction appears as an open circuit, yet the gate-to-source voltage affects the value of drain current. It is indicated by a voltage-controlled current source ($g_m \cdot v_{gs}$) whose value is proportional to the gate-to-source voltage. The FET transconductance (g_m) is measured in milliamperes per volt (mA/V), milli siemens (mS) or milli mhos (mΩ). Typical values of transconductance are from 0.5 mA/V to 10 mA/V for JFET's and 0.5 mA/V to 20 mA/V for MOSFET's.

The FET drain resistance (also called FET output resistance) is represented by the resistance (r_d). Typical values of drain resistance are from 100 kΩ to 1 MΩ for JFET's and 1 kΩ to 50 kΩ for MOSFET's.

3.4.2 Small-Signal High-Frequency FET Model

Figure 3.8 shows the small-signal high-frequency model of a field-effect transistor. It is identical to the low-frequency model, except the addition at capacitances between each pair of terminals. The capacitor, (c_{gs}) represents the barrier capacitance between the gate and source. Its typical value is from 1 pF to 10 pF for both JFET's and MOSFET's. The capacitor (C_{gd}) represents the barrier capacitance between the gate and drain. Its typical value is also from 1 pF to 10 pF for both JFET's and MOSFET's. Similarly, the capacitor (C_{ds}) represents the drain-to-source capacitance. The typical value of C_{ds} is from 0.1 pF to 1 pF.

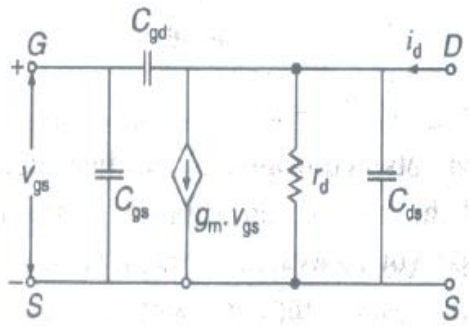


Fig. 3.8 High-frequency FET model.

3.5 Field Effect Transistor Amplifier

The field-effect transistor (FET) has a capability to amplify a.c. signals like a bipolar transistor. Depending open the configuration, the FET amplifiers may be studied under the following three heads:

1. Common source amplifier.
2. Common drain amplifier, and
3. Common gate amplifier.

3.5.1 Common Source Amplifier

Figure 3.9 shows the circuit of a common source N-channel JFET amplifier. It is similar to a common emitter amplifier. Here the resistors R_1 and R_2 (called a voltage divider) are used to bias the field-effected transistor. The capacitor (C_1) and (C_2) are used to couple the a.c. input voltage source and the output voltage respectively, these are known as coupling capacitors. The capacitor (C_S) keeps the source of the FET effectively at a.c. ground and is known as bypass capacitor.

The operation of the circuit may be understood from the assumption that when a small a.c. signal is applied to the gate, it produces variations in the gate-to-source voltage. This produces variations in the drain current.As the gate to source voltage

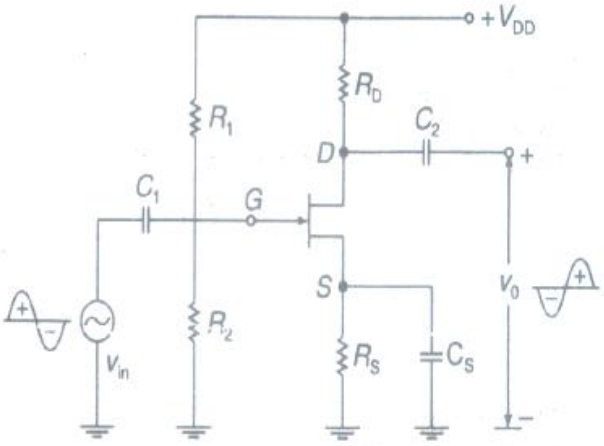


Fig. 3.9 Common Source Amplifier

increases, the drain current also increases. As a result of this, the voltage drop across the resistor (R_D) also increases. This causes the drain voltage to decrease. It means that the positive half cycle of the input voltage produces the negative half cycle of the output voltage. In other words, the output voltage (at the drain) is 180° out-of-phase with the input voltage (at the gate). This phenomenon of *phase inversion* is similar to that exhibited by a common emitter bipolar transistor amplifier.

3.5.1.1 Analysis of Common Source Amplifier

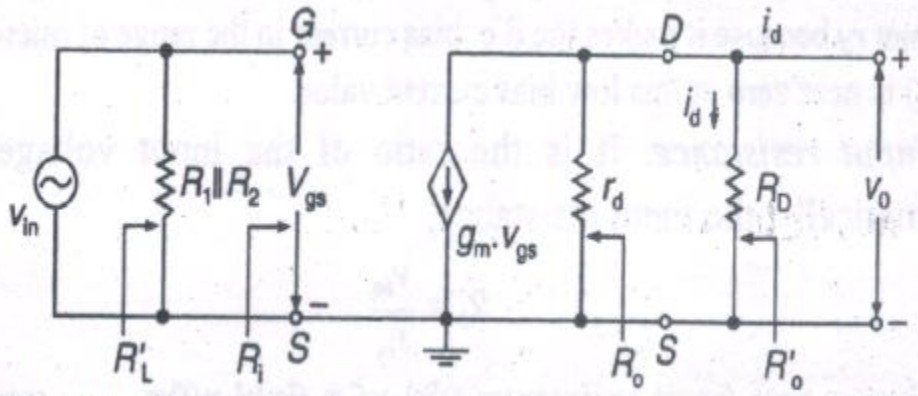


Fig. 3.10 A.C. equivalent circuit of a common source amplifier.

Figure 3.10 shows the a.c. equivalent circuit of a common source amplifier. This circuit has been obtained from the amplifier circuit shown in Figure 3.9 by short-circuiting the capacitors and the d.c. voltage supplies. The field-effect transistor is also replaced by its low-frequency model (or equivalent circuit). Now we shall use this circuit to find the expressions for amplifier voltage gain, *input resistance and output resistance.

1. *Voltage gain.* It is the ratio of the output voltage (v_o) to the input voltage (v_{in}). Mathematically the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

It may be noted that the current from the current source splits between the resistors r_d and R_D. The current through resistor R_D (as per current divider rule) is given by the relation,

$$i_d = \frac{r_d}{R_D + r_d}(g_m \cdot v_{gs})$$

and the output voltage,

$$v_o = -i_d \cdot R_D = -\left(\frac{r_d}{R_D + r_d}\right)(g_m \cdot v_{gs})\, R_D$$

$$= -g_m \left(\frac{r_d \cdot R_D}{R_D + r_d}\right) v_{gs}$$

$$= -g_m (r_d \parallel R_D) \cdot v_{gs}$$

$$= -g_m \cdot r_L \cdot v_{gs} \quad \ldots (\because r_L = r_d \parallel R_D)$$

$$= -g_m \cdot r_L \cdot v_{in} \quad \ldots (\because v_{in} = v_{gs})$$

The minus sign indicates that the output voltage is 180° out-of-phase with the input voltage.

∴ Voltage

$$A_v = \frac{v_o}{v_{in}} = -g_m \cdot r_L$$

It may be noted that if the drain resistance (r_d) is sufficiently greater than resistor R_D, (*i.e.*, $r_d \geq 10\, R_D$) then the equivalent resistance of the resistors r_d and R_D in parallel,

$$r_L = R_D$$

and the voltage gain,

$$A_v = g_m \cdot R_D$$

Note. If the resistance R_D is much larger than r_d (*i.e.*, $R_D >> r_d$) then a.c. load resistance (r_L) is approximately equal to r_d. In that case, the amplifier gain is equal to the FFT amplification factor (μ), which is the theoretical maximum voltage gain of the FET. But in actual practice, we cannot select R_D to be much larger than r_d because it makes the d.c. bias current in the range of microamperes. The FET transconductances (*i.e.*, g_m) is near zero at this low bias current value.

2. *Input resistance.* It is the ratio of the input voltage (v_{in}) to the input current (i_{in}). Mathematically, the input resistance,

$$R_i = \frac{v_{in}}{i_{in}}$$

We know that input resistance (R_i) of a field-effect transistor is very high and hence can be considered to be infinity (*i.e.*, open-circuit). However, the input resistance of the amplifier stage (R'_i) is equal to the parallel combination of resistors R_1 and R_2 and the FET input resistance (R_i). Thus

$$R'_i = (R_1 \parallel R_2) \parallel R_i$$

$$= R_1 \parallel R_2 \quad \ldots \text{(When } R_i \text{ is infinite)}$$

It may be noted that if we use a self-bias circuit (instead of a voltage divider bias), then the input resistance of the amplifier stage,

$$R'_i = R_G$$

3. *Output resistance.* It is the ratio of the output voltage (v_o) to the output current (i_d). Mathematically, the output resistance,

$$R'_o = \frac{v_o}{i_d}$$

We know that the output resistance (R_o) of a field-effect transistor is r_d. But for the amplifier stage, the output resistance is the parallel combination of resistors R_D and r_d. *i.e.*,

$$R'_o = R_D \parallel r_d$$

However, if $r_d >> R_D$, then the output resistance of amplifier stage,

$$R_o = R_D$$

Example *A certain JFET has a g_m of 4 mS. With an external drain resistance of 1.5 kΩ, find the value of ideal voltage gain.*

Solution. Given: $g_m = 4 \text{ mS} = 4 \times 10^{-3} \text{ S}$ and $R_D = 1.5 \text{ k}\Omega = 1.5 \times 10^3 \Omega$.

We know that the voltage gain,

$$A_v = -g_m \cdot R_D = -(4 \times 10^{-3}) \times (1.5 \times 10^3) = -6 \textbf{ Ans.}$$

Example *A JFET amplifier has $g_m = 2.5$ mA/V and $r_d = 500$ kΩ. The load resistance is 10 kΩ. Find the value of voltage gain.*

Solution. Given: $g_m = 2.5 \text{ mA/V} = 2.5 \times 10^{-3} \text{ A/V}$;

$r_d = 500 \text{ k}\Omega$ and $R_D = 10 \text{ k}\Omega$.

We know that the a.c. equivalent resistance,

$$r_L = \frac{R_D \times r_d}{R_D + r_d} = \frac{10 \times 500}{10 + 500} \text{ k}\Omega = 9.8 \text{ k}\Omega = 9.8 \times 10^3 \Omega$$

$\therefore$ Voltage gain,

$$A_v = -g_m \cdot r_L = -(2.5 \times 10^{-3}) \times (9.8 \times 10^3)$$
$$= -24.5 \textbf{ Ans.}$$

Example *The input and output resistances of the FET amplifier are shown in Figure Calculate the value of voltage gain. The FET amplifier has $g_m = 2$ mA/V and $r_d = 40$ kΩ.*

Solution. Given: $g_m = 2$ mA/V $= 2 \times 10^{-3}$ A/V; $r_d =$ 40 kΩ; $R_D = 20$ kΩ and $R_G = 100$ MΩ.

Voltage gain

We know that the a.c. equivalent resistance,

$$r_L = \frac{R_D \times r_d}{R_D + r_d} = \frac{20 \times 40}{20 + 40} = 13.3 \text{ k}\Omega$$

$$= 13.3 \times 10^3 \ \Omega$$

∴ Voltage gain

$$A_v = -g_m \cdot r_L = -(2 \times 10^{-3}) \times (13.3 \times 10^3) = -26.7 \textbf{ Ans.}$$

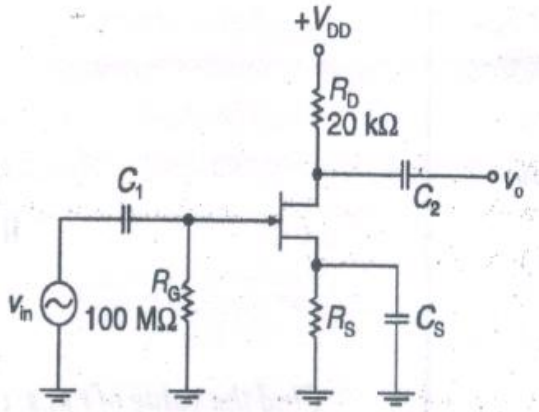


Fig.

Input resistance

We know that the input resistance,

$$R'_i = R_G = 100 \text{ M}\Omega \textbf{ Ans.}$$

Outpur resistance

We also know that the output resistance,

$$R_o' = r_L = 13.3 \text{ k}\Omega \textbf{ Ans.}$$

3.5.1.2 Effect of A.C. Load on Amplifier Parameters

Consider a common source amplifier shown in Figure 3.11. Here a load resistance (R_L) is connected to the amplifier's output through a coupling capacitor. In this case, the total or effective drain resistance is the parallel combination of resistors R_D and R_L *i.e.*,

$$r_L = R_D \parallel R_L$$

It may be noted that in the above expression, if we also consider the FET drain resistance (r_d), then the effective drain resistance,

$$r_L = (R_D \parallel R_L) \parallel r_d$$

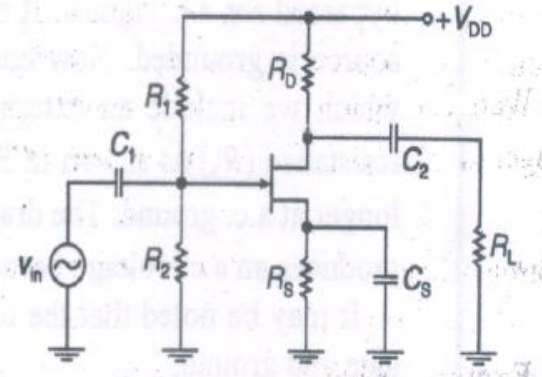


Fig. 3.11. Common source amplifier connected to a load resistor.

The effect of load resistor (R_L) is to reduce the voltage gain as well as the output resistance. The value of voltage gain with load resistance is given by the relation,

$$A_v = -g_m \cdot r_L$$
$$= -g_m (R_D \parallel R_L) \parallel r_d$$
$$= -g_m (R_D \parallel R_L) \quad \text{... (If } r_d >> (R_D \parallel R_L))$$

and the output resistance, of the amplifier stage

$$R'_o = (R_D \parallel R_L) \parallel r_d$$
$$= R_D \parallel R_L \quad \text{... (If } r_d >> (R_D \parallel R_L))$$

3.5.1.3 Effect of External Source Resistance on Voltage Gain

We have already discussed a field-effect transistor amplifier in which the source resistor is completely bypassed for a.c. signals. It means that for a.c. signals, the source is grounded. Now consider the amplifier circuit in which we include an external resistor (V_S) to the source resistance (R_S) as shown in Figure 3.12. The source is no longer at a.c. ground. The drain current through resistor (r_S) produces an a.c. voltage between the source and ground.

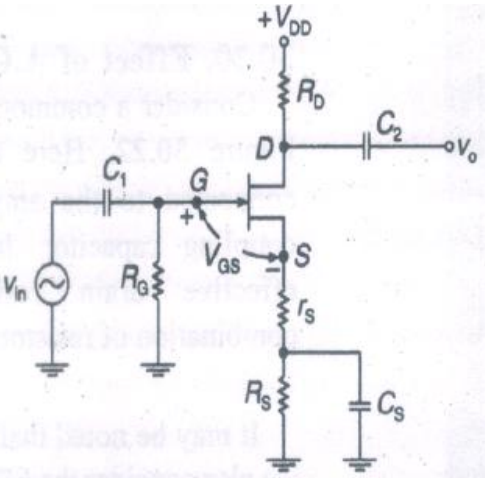


Fig. 3.12. JFET amplifier with external source resistance.

It may be noted that the total input voltage between the gate and ground,

$$v_{in} = v_{gs} + i_d \cdot r_s$$

and the output voltage,

$$v_o = -i_d \cdot r_L$$

where r_L is the parallel combination of resistor R_D and the FET output resistance (r_d). Therefore voltage gain,

$$A_v = \frac{v_o}{v_{in}} = -\frac{i_d \cdot r_L}{v_{gs} + i_d \cdot r_s}$$

Substituting the value of i_d (equal to $g_m \cdot v_{gs}$) in the above expression,

$$A_v = -\frac{g_m \cdot v_{gs} \cdot r_L}{v_{gs} + g_m \cdot v_{gs} \cdot r_s} = -\frac{g_m \cdot v_{gs} \cdot r_L}{v_{gs}(1 + g_m \cdot r_s)} = -\frac{g_m \cdot r_L}{1 + g_m \cdot r_s} = \frac{r_L}{r_s + \frac{1}{g_m}}$$

It is evident from the above expression that the external source resistance (r_s) reduces the voltage gain. If the value of resistor r_s is made sufficiently large as compared to $1/g_m$, then the voltage gain,

$$A_v = -\frac{r_L}{r_s}$$

It means that the voltage gain is independent of the changes in the transconductance value. It is known as the swamping effect. Because of this fact the external source resistance (r_s) is referred to as the swamping resistor and the FET amplifier as the swamped amplifier.

Example *Figure shows the circuit of a swamped FET amplifier. Determine the voltage gain (a) when $R_L = 0$ and (b) when R_L is 100 kΩ. Neglect the FET output resistance (r_d) Take $g_m = 4$ mS.*

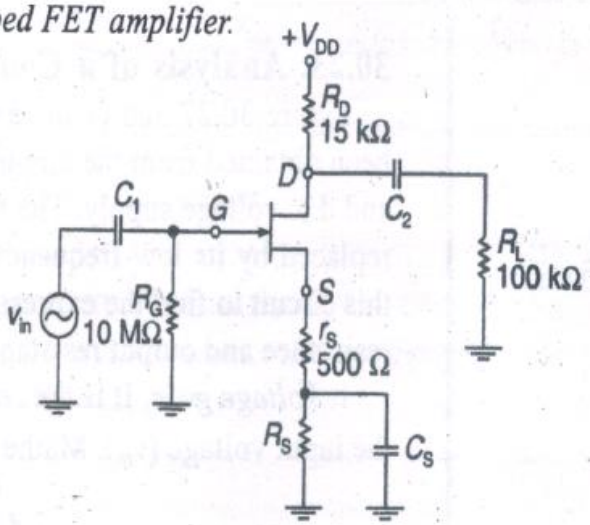


Fig.

Solution. Given: $g_m = 4$ mS $= 4 \times 10^{-3}$ S; $R_D = 1.5$ kΩ; $R_G = 10$ MΩ and $r_s = 500$ Ω.

(a) Voltage gain when R_L is zero

We known that the effective a.c. drain resistance,

$$r_L = R_D = 1.5 \times 10^3\ \Omega$$

and the voltage gain,

$$A_v = -\frac{g_m \cdot r_L}{1 + g_m \cdot r_s}$$

$$= -\frac{(4 \times 10^{-3}) \times (1.5 \times 10^3)}{1 + (4 \times 10^{-3}) \times 500} = -2 \text{ Ans.}$$

(b) Voltage gain when R_L is 100 kΩ

We know that the effective a.c. drain resistance,

$$r_L = \frac{R_D \times R_L}{R_D + R_L} = \frac{1.5 \times 100}{1.5 + 100} = 1.48\ \text{k}\Omega = 1.48 \times 10^3\ \Omega$$

and the voltage gain,

$$A_v = -\frac{g_m \cdot r_L}{1 + g_m \cdot r_s}$$

$$A_v = -\frac{(4 \times 10^{-3}) \times (1.48 \times 10^3)}{1 + (4 \times 10^{-3}) \times 500}$$
$$= -1.97 \textbf{ Ans.}$$

3.6 Common Drain Amplifier

Figure 3.13 shows the circuit of a common drain amplifier. It is similar to common collector (or emitter follower) amplifier. Self-biasing is used in the circuit. The input signal is applied to the gate through a coupling capacitor (C_1). And the output is taken from the source terminal through the coupling capacitor (C_2).

The operation of the amplifier may be understood by assuming that when a small a.c. signal is applied to the gate, it produces variations in the gate to source voltage.This further produces the variations in drain current (I_D). As the gate-to-source voltage increases, the drain current also increases. As a result of this, the voltage drop across the source resistor (R_S) also increases. Thus the output voltage (v_o) increases. It may be noted that the output voltage of a common drain amplifier is approximately equal to and in phase with the input voltage. Because of this fact, the circuit is known as source follower.

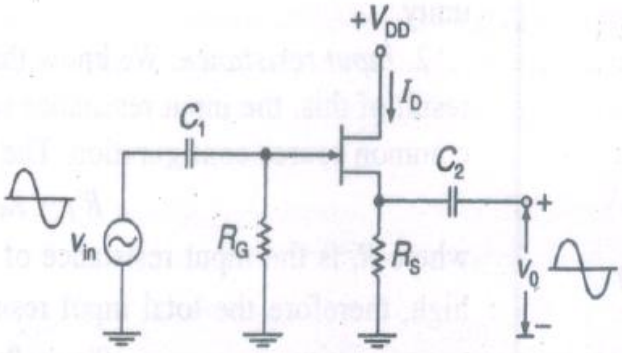


Fig. 3.13 Common Drain Amplifier

A common drain amplifier (or a source follower) has a very high value of input resistance. It is because of this property that a common drain amplifier is used at the front end of measuring instruments like electronic voltmeters and cathode ray oscilloscopes.

3.6.1 Analysis of a Common Drain Amplifier

Figure 3.14 shows the a.c. equivalent circuit of a common drain amplifier. This circuit has been obtained from the amplifier circuit shown in Figure 3.13 by short circuiting the capacitors and d.c. voltage supply. The field-effect transistor is also replaced by its low-frequency model. Now we shall use this circuit to find the expressions for voltage gain, input resistance and output resistance.

1. *Voltage gain.* It is the ratio of output voltage (v_o) to the input voltage (v_{in}). Mathematically, the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

For the common drain amplifier, the input voltage,

$$v_{in} = v_{gs} + i_d \cdot R_s$$

and the output voltage,

$$v_o = i_d \cdot R_S$$

∴ Voltage gain,

$$A_v = \frac{v_o}{v_{in}} = \frac{i_d \cdot R_s}{v_{gs} + i_d \cdot R_s}$$

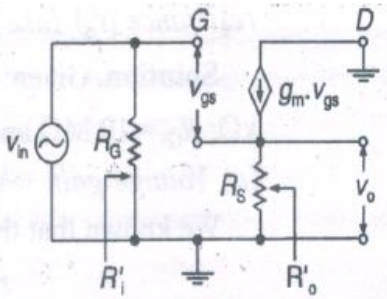


Fig. 3.14 A.C. equivalent circuit of a common drain amplifier.

Substituting the value of i_d ($= g_m \cdot v_{gs}$) in the above expression,

$$A_v = \frac{(g_m \cdot v_{gs})\, R_s}{v_{gs} + g_m \cdot v_{gs} \cdot R_s}$$

$$= \frac{g_m \cdot v_{gs} \cdot R_s}{v_{gs}\,(1 + g_m \cdot R_s)}$$

$$= \frac{g_m \cdot R_s}{1 + g_m \cdot R_s} = \frac{R_s}{R_s + \dfrac{1}{g_m}}$$

It may be noted that when R_s is much greater than $1/g_m$, the value of voltage gain approaches unity.

2. *Input resistance.* We know that the input signal is applied to the gate of the amplifier. As a result of this, the input resistance seen by the input signal source is extremely high just as in the common source configuration. The total input resistance (or the input resistance of the amplifier),

$$R'_i = R_G \parallel R_i$$

where R_i is the input resistance of the field effect transistor. Since the value of R_i is extremely high, therefore the total input resistance,

$$R'_i = R_G$$

3. *Output resistance.* We know that voltage gain of the common drain amplifier,

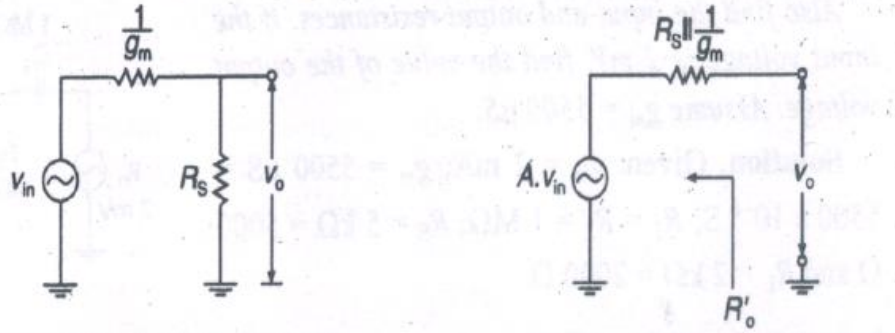
$$A_v = \frac{v_o}{v_{in}} = \frac{R_s}{R_s + \dfrac{1}{g_m}}$$

∴ Output voltage,

$$v_o = \left(\frac{R_s}{R_s + \dfrac{1}{g_m}} \right) \times v_{in}$$

The above expression is a voltage-divider equation. It implies that the input voltage (v_{in}) drives two resistors R_s and $1/g_m$ with output voltage taken across resistor (R_s). It means that the output side of the amplifier appears as shown in Figure 3.15(a). It is evident from this figure, that the source resistor is driven by an a.c. source with an output resistance *i.e.*,

$$R_D = 1/g_m$$



(*a*) A.C. equivalent circuit of output side of the amplifier.

(*b*) Thevenin's equivalent circuit of the amplifier.

Fig. 3.15

It may be noted that output resistance (R_o) is the value of resistance looking back into the source terminal of the JFET. Now let us thevenize the output circuit. The resulting circuit is as shown in Figure 3.15 (b). It is evident from this figure, that the resistance R_s is in parallel with $1/g_m$ and the output resistance of the amplifier stage,

$$R'_o = R_s \| \frac{1}{g_m}$$

If the value of source resistance (R_s) is much larger than $1/g_m$, then the output resistance of the amplifier stage,

$$R'_o = \frac{1}{g_m}$$

Example *Figure shows the circuit of a source follower. Determine the voltage gain of the amplifier.*

Also determine the input and output resistance of the amplifier. Assume g_m = 800 μS, infinite input resistance and neglect FET output resistance.

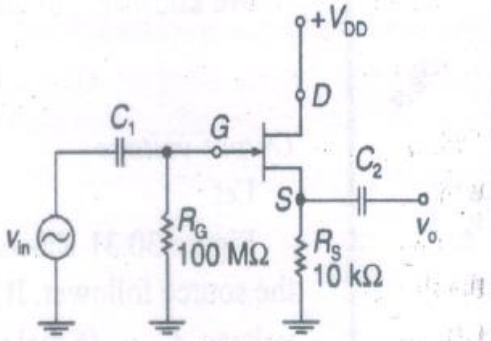


Fig.

Solution. Given: $g_m = 8000\ \mu S = 8000 \times 10^{-6}$ S;

$R_G = 10\ k\Omega = 10 \times 10^3\ \Omega$ and $R_G = 100\ M\Omega$.

Voltage gain

We know that the reciprocal of transconductance,

$$\frac{1}{g_m} = \frac{1}{8000 \times 10^{-6}} = 125\ \Omega \textbf{ Ans.}$$

and the voltage gain,

$$A_v = \frac{R_s}{R_s + \frac{1}{g_m}} = \frac{10 \times 10^3}{(10 \times 10^3) + 125} = 0.988 \textbf{ Ans.}$$

Input resistance

We know that the input resistance

$$R'_i = R_G = 100\ \text{M}\Omega \textbf{ Ans.}$$

Output resistance

We also know that the output resistance,

$$R'_o = \frac{1}{g_m} = \frac{1}{8000 \times 10^{-6}} = 125\ \Omega \textbf{ Ans.}$$

Example *Find the voltage gain for the source follower shown in Figure*

Also find the input and output resistances. If the input voltage is 2 mV, find the value of the output voltage. Assume $g_m = 5500\ \mu S$.

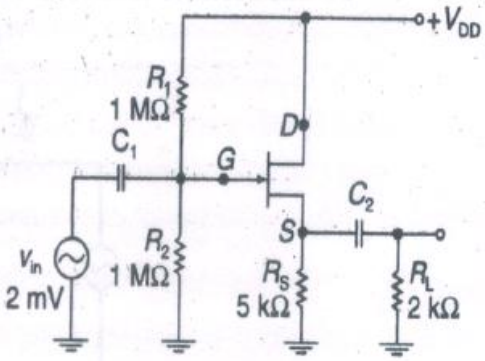


Fig.

Solution. Given: $v_{in} = 2$ mA; $g_m = 5500\ \mu S = 5500 \times 10^{-6}$ S; $R_1 = R_2 = 1\ \text{M}\Omega$; $R_S = 5\ \text{k}\Omega = 5000\ \Omega$ and $R_L = 2\ \text{k}\Omega = 2000\ \Omega$.

Voltage gain

We know that the reciprocal of transconductance,

$$\frac{1}{g_m} = \frac{1}{5500 \times 10^{-6}} = 181.8\ \Omega$$

and the voltage gain,

$$A_v = \frac{R_s}{R_s + \frac{1}{g_m}} = \frac{5000}{5000 + 181.8} = 0.965 \textbf{ Ans.}$$

Input resistance

We know that input resistance,

$$R'_i = R_1 \| R_2 = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{1 \times 1}{1+1} \text{ M}\Omega = 0.5 \text{ M}\Omega \textbf{ Ans.}$$

Output resistance

We know that the input resistance,

$$R'_o = R_s \| \frac{1}{g_m} = 5000 \| 181.8 = 175.4 \ \Omega \textbf{ Ans.}$$

Output voltage

Let v_o = Value of the output voltage.

Figure 3.16 shows the a.c. equivalent circuit of the output side of the source follower. It is evident from this figure, that an a.c. source of voltage $A_v \cdot v_{in}$ (equal to 0.965 × 2 or 1.93 V) is in series with an output resistance of 175.4 Ω.

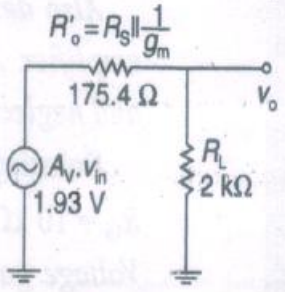


Fig. 3.16

We know that the a.c. voltage across the load resistor,

$$= \left(\frac{R_L}{R_L + R'_o} \right) \times A_V.v_{in}$$

$$= \left(\frac{2000}{2000 + 175.4} \right) \times 1.93 \text{ mV}$$

$$= 1.77 \text{ mV } \textbf{Ans.}$$

3.7 Common Gate Amplifier

Figure 3.17 shows the circuit of a common gate amplifier. It is similar to a common base amplifier. The input signal is applied at the source through a coupling capacitor (C_1) and the output is taken from the drain through the coupling capacitor (C_2). The gate is effectively at a.c. ground because of the capacitor, (C_G).

The operation of the common gate amplifier may be understood from the assumption that when a small a.c. signal is applied to the source, it produces variation in gate-to-source voltage (V_{GS}). This inturn, produces the variations in drain current (I_D). As the gate-to-source voltage increases, the drain current also increases. As a result of this, the output voltage also increases. Thus output voltage of a common gate amplifier is in phase with the input voltage.

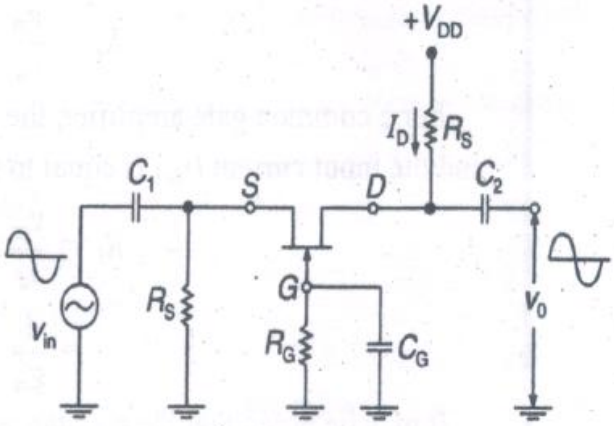


Fig. 3.17 Common gate amplifier.

A common gate amplifier has a low input resistance, high output resistance, high voltage gain and no phase reversal.

3.7.1 Analysis of a Common Gate Amplifier

Figure 3.18 shows an a.c. equivalent circuit of a common gate amplifier. This circuit has been obtained from the amplifier circuit shown in Figure 3.17 by short-circuiting the capacitors and the d.c. supply. The field-effect-transistor is also replaced by its low-frequency model.

Now we shall use this circuit to find the expressions for amplifier voltage gain, input resistance and output resistance.

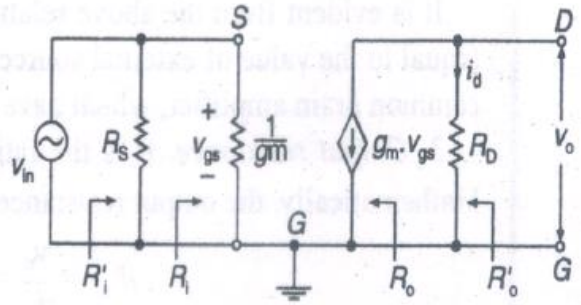


Fig. 3.18. Common gate amplifier.

1. *Voltage gain.* It is the ratio of a.c. output voltage (v_o) to the a.c. input voltage (v_{in}). Mathematically, the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

We know that the a.c. input voltage,

$$v_{in} = v_{gs}$$

and the a.c. output voltage,

$$v_o = i_d \cdot R_D$$

$\therefore$ Voltage gain, $$A_v = \frac{i_d \cdot R_D}{v_{gs}}$$

Substituting the value of i_d (equal to $g_m \cdot v_{gs}$) in the above expression,

$$A_v = \frac{(g_m \cdot v_{gs}) \cdot R_D}{v_{gs}} = g_m \cdot R_D$$

It may be noted that the above expression for voltage gain is true only when there is no load resistor. If there is a load resistor (R_L) connected to the amplifier output, then the voltage gain.

$$A_v = g_m (R_D \parallel R_L)$$

2. *Input resistance.* It is the ratio of input voltage (v_{in}) to the input current (i_{in}). Mathematically, the input resistance,

$$R_i = \frac{v_{in}}{i_{in}}$$

For a common gate amplifier, the input voltage (v_{in}) is equal to the gate-to-source voltage (v_{gs}) and the input current (i_{in}) is equal to the drain current (i_d). Therefore the input resistance,

$$R_i = \frac{v_{gs}}{i_d} = \frac{v_{gs}}{g_m \cdot v_{gs}} \quad \ldots (\because \; i_d = g_m \cdot v_{gs})$$

$$= \frac{1}{g_m}$$

It may be noted that the resistance (R_i) is the value of input resistance looking directly into the source terminal of the JFET. The input resistance of the amplifier,

$$R'_i = R_s \parallel \frac{1}{g_m}$$

However, if R_s is much larger than the reciprocal of tranconductance ($1/g_m$) then the input resistance of the amplifier,

$$R'_i = R_s$$

It is evident from the above relation that a common gate amplifier has a low input resistance (equal to the value of external source resistance only). It is in contrast to the common source and common drain amplifier, which have extremely high input resistances.

3. *Output resistance.* It is the ratio of a.c. output voltage (v_o) to the a.c. output current (i_o). Mathematically, the output resistance of the amplifier,

$$R'_o = \frac{v_o}{i_o} = \frac{i_d \cdot R_D}{i_d} \quad \ldots (\because \; v_o = i_d \cdot R_D \text{ and } i_o = i_d)$$

$$= R_D$$

It means that the output resistance of the common gate amplifier is equal to the external drain resistance (R_D). If there is a load resistor (R_L) connected to the amplifier output, then the output resistance of the amplifier,

$$R'_o = R_D \| R_L$$

Example *Figure shows the circuit of a common gate JEET amplifier. The JFET has transconductance $g_m = 2500$ μS.*

Determine the amplifier voltage gain and input resistance.

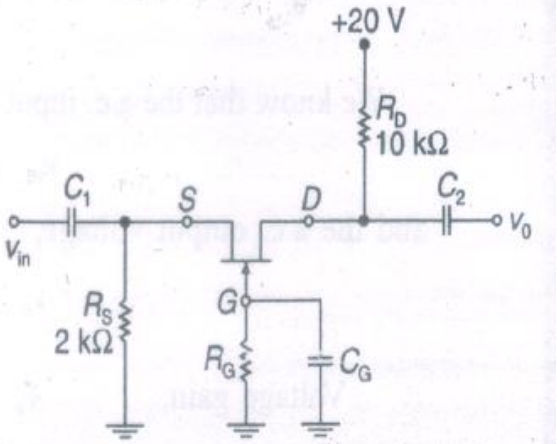


Fig.

Solution. Given: $g_m = 2500\ \mu S = 2500 \times 10^{-6} S$; $R_D = 2\ k\Omega = 2000\ \Omega$ and $R_D = 10\ k\Omega = 10{,}000\ \Omega$.

Voltage gain

We know that voltage gain,

$$Av = g_m \cdot R_D = 2500 \times 10^{-6} \times 10{,}000 = 25$$

Input resistance

We know that reciprocal of transconductance,

$$\frac{1}{g_m} = \frac{1}{2500 \times 10^{-6}} = 400\ \Omega$$

and the amplifier input resistance,

$$R'_i = R_i \| \frac{1}{g_m} = 2000 \| 400\ \Omega$$

$$= \frac{2000 \times 400}{2000 + 400} = 333\ \Omega \textbf{ Ans.}$$

Example *For a JFET, the transconductance at zero gate-to-source voltage, $g_{mo} = 5$ mS. Determine the amplifier input resistance (R'_i) and a.c. voltage gain (v_o/v_{in}) for the circuit shown in Figure · Assume the capacitors to be short circuit for a.c.*

Solution. Given: $g_{mo} = 5$ mS $= 5 \times 10^{-3}$ S; $R_D = 1$ kΩ $= 1 \times 10^3$ Ω; $R_s = 200$ Ω and $I_D = 5$ mA $= 5 \times 10^{-3}$ A.

Input resistance

We know that reciprocal of transconductance

$$\frac{1}{g_{mo}} = \frac{1}{5 \times 10^{-3}} = 200 \ \Omega$$

and the input resistance of the amplifier,

$$R'_i = R_s \| \frac{1}{g_{mo}} = 200 \| 200 \ \Omega = 100 \ \Omega \text{ Ans.}$$

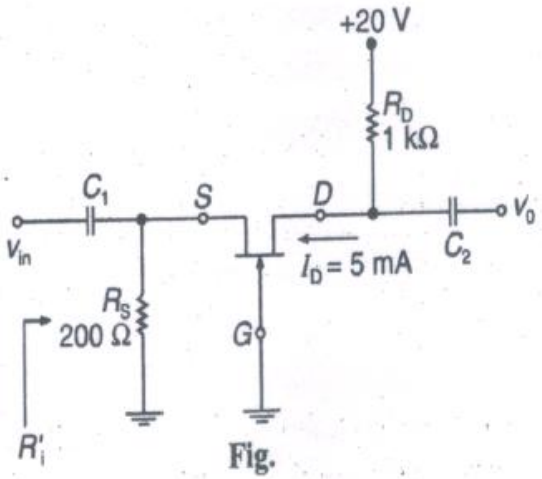


Fig.

Voltage gain

We know that the d.c. source voltage,

$$V_S = I_D \cdot R_S = (5 \times 10^{-3}) \times 200 = 1 \text{ V}$$

and the gate-to-source voltage,

$$V_{GS} = V_S = 1 \text{ V}$$

We also know that the *maximum value of drain current,

$$I_{DSS} = 2 I_D = 2 \times (5 \times 10^{-3}) = 10 \times 10^{-3} \text{ A}$$

and gate-to-source cut-off voltage

$$V_{GS\,(off)} = -\frac{2 I_{DSS}}{I_D} = -\frac{2 \times (10 \times 10^{-3})}{5 \times 10^{-3}} = -4 \text{ V}$$

and the transconductance (g_m)

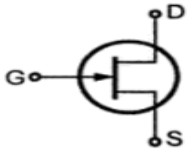
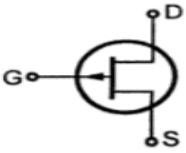
$$= g_{mo}\left[1 - \frac{V_{GH}}{V_{GS\,(off)}}\right]$$

$$= (5 \times 10^{-3})\left[1 - \frac{1}{4}\right]$$

$$= 3.75 \times 10^{-3} \text{ S}$$

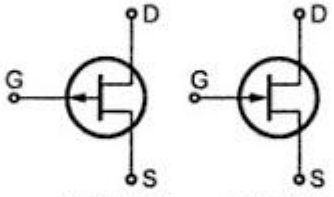
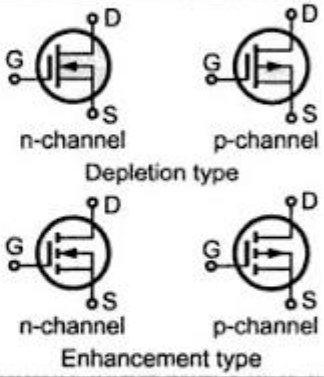
3.8 Comparison of n-channel and p-channel JFET

Table 2. Comparison of n-channel and p-channel JFET

Sr. No.	n-channel JFET	p-channel JFET
1.	Symbol 	Symbol 
2.	Electrons are the current carriers.	Holes are the current carriers.
3.	Mobility of electrons is large in n-channel JFET.	Mobility of holes is poor in p-channel JFET.
4.	Input noise is less.	Input noise is more.
5.	Large transconductance.	Less transconductance.

3.9 Comparison of JFET and MOSFET

Table 3. Comparison of JFET and MOSFET

Sr. No.	Parameter	JFET	MOSFET
1.	Types	a) n-channel b) p-channel	A)n-channel depletion type MOSFET B)p-channel depletion type MOSFET C)n-channel enhancement type MOSFET D)p-channel enhancement type MOSFET
2.	Symbols		
3.	Operation mode	Operated in depletion mode.	Operated in depletion and enhancement mode.
4.	Input impedance	High (> 10 MHz)	Very high (> 10,000 MΩ)
5.	Gate	Gate is not insulated from channel.	Gate is insulated from channel by a layer of SiO_2.
6.	Channel	Channel exists permanently .	Channel exists permanently in depletion type MOSFET, but not in enhancement type MOSFET.

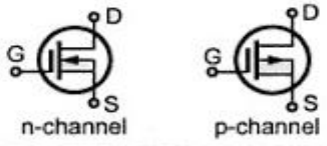
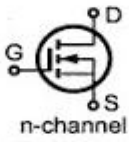
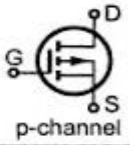
3.10 Introduction to MOSFET

MOSFET (metal oxide semiconductor field effect transistor). It is a second category of field effect transistor. It became a practical reality in the 1970s. The MOSFETs, compared to BJTs, can be made very small and hence can be used to design high density VLSI circuits.

The MOSFET differs from the JFET in that it has no p-n junction structure ; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input resistance of MOSFET is greater than JFET. Because of the insulated gate, MOSFETs are also called **IGFETs**. The two basic types of MOSFETs are : depletion (D) MOSFET and enhancement (E) MOSFET.

3.11 Comparison of D-MOSFET and E-MOSFET

Table 4. Comparison of D-MOSFET and E-MOSFET

Sr. No	Parameter	Depletion type	Enhancement type
1.	Symbols	 n-channel p-channel	 n-channel  p-channel
2.	Channel	Exists permanently.	Channel is physically absent. It is induced after application of positive gate voltage above the threshold value for n-channel enhancement type MOSFET and negative gate voltage above threshold value for p-channel enhancement type MOSFET.
3.	Operation	Can be operated in depletion mode as well as enhance mode.	Can only be operated in enhance mode.
4.	Current flow	Drain current flows on application of drain to source voltage, at $V_{GS} = 0$.	Practically no current flows on application of drain to source, at $V_{GS} = 0$. Current flows only when V_{GS} is above threshold level.

3.12 Biasing Circuits for MOSFET

There are two biasing circuits for MOSFET namely D-MOSFET AND E-MOSFET.

3.12.1 Biasing Circuits for D-MOSFET

Biasing circuits for depletion type MOSFET are quite similar to the circuits used for JFET biasing. The primary difference between the two is the fact that depletion type MOSFETs also permit operating points with positive value of V_{GS} for n-channel and negative values of V_{GS} for p-channel MOSFET. To have positive value of V_{GS} for n-channel and negative value of V_{GS} for p-channel self bias circuit is unsuitable.

3.12.2 Biasing Circuits for E-MOSFET

Biasing circuits for enhancement type MOSFET are similar to the circuit used for JFET biasing. The primary difference between two is the fact that enhancement type MOSFET only permits operating points with positive value of V_{GS} for n channel and negative value of V_{GS} for p-channel. To have positive value of V_{GS} for n channel and negative value of V_{GS} for p channel self bias circuit is unsuitable. Thus we discuss feedback bias and voltage divider circuits for enhancement type MOSFET.

3.12.2.1. Feedback Circuit Bias

Fig. 3.19 shows the feedback bias circuit for n-channel enhancement type MOSFET.

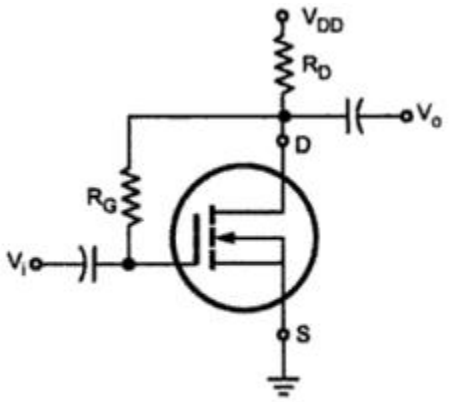


Fig. 3.19 Feedback bias circuit

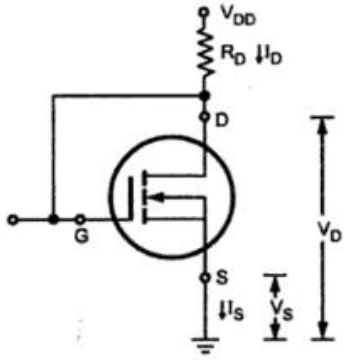


Fig. 3.20 Simplified feedback bias circuit for d.c. analysis

As mentioned earlier, for d.c. analysis we can replace coupling capacitors by open circuits and we also replace the register R_G by a short circuit equivalent, since $I_G = 0$ Fig. 3.56 shows simplified circuit with feedback bias for dc analysis.

As drain and gate terminals are shorted

$$V_D = V_G$$

and $$V_{DS} = V_{GS} \quad \because V_S = 0 \ldots (13)$$

Applying KVL to output circuit we get,

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\therefore \quad V_{DS} = V_{DD} - I_D R_D \ldots (14)$$

$$\text{or} \quad V_{GS} = V_{DD} - I_D R_D \quad \because V_{DS} = V_{GS} \ldots (15)$$

Example : *For the given circuit in Fig. Calculate V_{GS}, I_D and V_{DS}.*

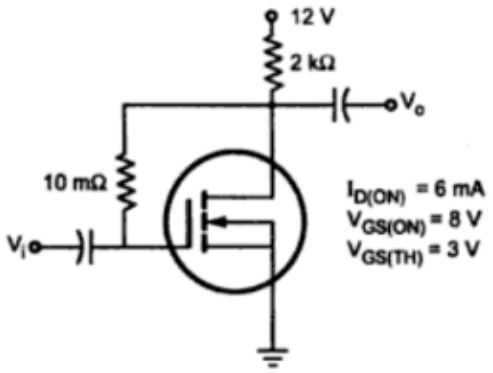


Fig.

Solution :

We have, $$K = \frac{I_{D(ON)}}{(V_{GS(on)} - V_T)^2} = \frac{6\times 10^{-3}}{(8-3)^2} = 0.24\times 10^{-3}\ A/V^2$$

$$V_{GS} = V_{DD} - I_D R_D = 12 - I_D R_D$$

We have, $$I_D = K(V_{GS} - V_T)^2$$

Substituting value of V_{GS} we get,

$$I_D = K((12 - I_D R_D) - V_T)^2 = 0.24\times 10^{-3}\,[12 - I_D \times 2\times 10^3 - 3]^2$$

$$= 0.24\times 10^{-3}\,[9 - 2000\, I_D]^2$$

$$= 0.24\times 10^{-3}[81 - 36000\, I_D + 4000000\, I_D^2]$$

$$\therefore\ I_D = 0.01944 - 8.64\, I_D + 960\, I_D^2$$

$$\therefore\ 960\, I_D^2 - 9.64\, I_D + 0.01944 = 0$$

Solving quadratic equation using formula $\frac{-b\pm\sqrt{b^2 - 4ac}}{2a}$ we get,

$$= \frac{-(-9.64)\pm\sqrt{(-9.64)^2 - 4(960)(0.01944)}}{2(960)}$$

$$= \frac{+9.64\pm\sqrt{18.28}}{1920}$$

$$= \frac{+9.64\pm 4.2755}{1920} = 2.794\ mA \text{ or } 7.2477\ mA$$

If we calculate value of V_{DS} taking $I_D = 7.2477$ mA we get,

$$V_{DS} = V_{DD} - I_D R_D = 12 - 7.2477 \times 10^{-3} \times 2 \times 10^3$$

$$= 12 - 14.495 = -2.495$$

Practically, the value of V_{DS} must be positive, hence $I_D = 7.2477$ mA is invalid.

Now, calculating value of V_{DS} taking $I_D = 7.2477$ mA,0

$$V_{DS} = 12 - 2.794 \times 10^{-3} \times 2 \times 10^3 = 12 - 5.588 = 6.412 \text{ V}$$

$$\therefore V_{GS} = 6.412 \text{ V}$$

3.12.2.2 Voltage Divide Bias

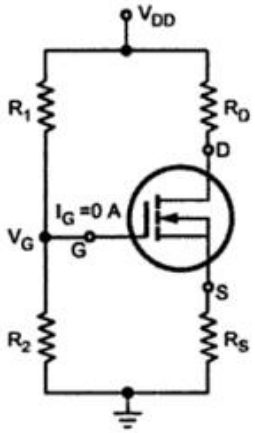


Fig. 3.21

Fig. 3.21 shows voltage divider bias for n-channel enhancement type MOSFET. It is similar to voltage divider bias provided for JFET and depletion type MOSFET. The only difference is biasing resistors R_1 and R_2 are designed to provide positive gate to source voltage.

D.C. Analysis :

As $I_G = 0$ A

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \quad \ldots (16)$$

Applying KVL to input circuit we get,

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - I_S R_S = V_G - I_D R_S \quad \because I_D = I_S$$

$$\therefore V_{GS} = V_G - I_D R_S \quad \ldots (17)$$

Applying KVL to output circuit we get,

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_S R_S = V_{DD} - I_D R_D - I_D R_S \quad \because I_D = I_S$$

$$= V_{DD} - I_D (R_D + R_S) \quad \ldots (18)$$

Example : *For the circuit shown in Fig. Calculate V_G, I_D, V_{GS} and V_{DS}.*

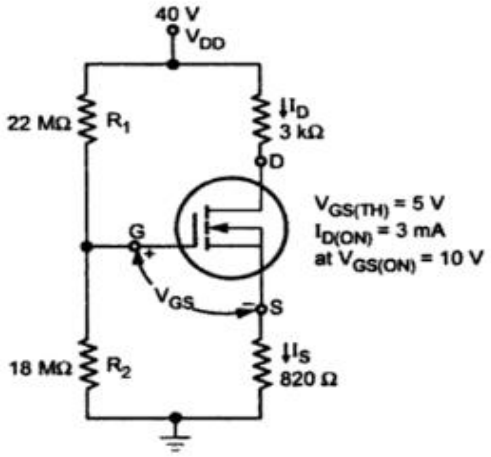


Fig.

Solution : From equation (4) we have,

$$V_G = \frac{V_{DD}\, R_2}{R_1 + R_2} = \frac{40 \times 18}{18 + 22} = 18 \text{ V}$$

From equation (5) we have,

$$V_{GS} = V_G - I_D R_S = 18 - I_D R_S$$

From equation (2) we have,

$$K = \frac{I_{D(ON)}}{\left(V_{GS(ON)} - V_{GS(TH)}\right)^2} = \frac{3 \times 10^{-3}}{(10-5)^2} = 0.12 \times 10^{-3} \text{ A/V}^2$$

We have, $$I_D = K\left(V_{GS} - V_{GS(TH)}\right)^2$$

Substituting value of V_{GS} we get,

$$I_D = K\left(18 - I_D R_S - V_{GS(TH)}\right)^2 = 0.12 \times 10^{-3} (18 - 820\, I_D - 5)^2$$

$$= 0.12 \times 10^{-3} (13 - 820\, I_D)^2 = 0.12 \times 10^{-3} (169 - 21320\, I_D + 672400\, I_D^2)$$

$$\therefore I_D = 0.02028 - 2.5584\, I_D + 80.688\, I_D^2$$

$$\therefore 80.688\, I_D^2 - 3.5584\, I_D + 0.02028 = 0$$

Solving quadratic equation using formula $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$ we get,

$$= \frac{-(-3.5584) \pm \sqrt{(-3.5584)^2 - 4\,(80.688)\,(0.02028)}}{2\,(80.688)} = \frac{3.5584 \pm 2.4732}{161.376}$$

$$= 37.38 \text{ mA or } 6.725 \text{ mA}$$

If we calculate value of V_{DS} taking $I_D = 37.38$ mA we get,

$$V_{DS} = V_{DD} - I_D\,(R_D + R_S) = 40 - 37.38 \times 10^{-3}\,(3 \times 10^3 + 820)$$

$$= 40 - 142.8 = -102.8 \text{ V}$$

Practically, the value of V_{DS} must be positive, hence $I_D = 37.38$ mA is invalid. Now, calculating value of V_{DS} taking $I_D = 6.725$ mA,

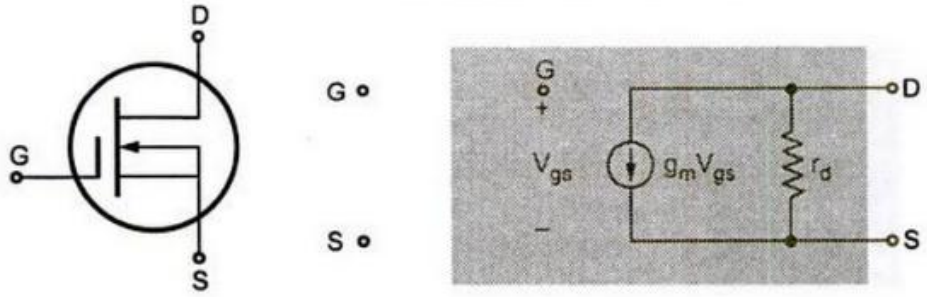
$$V_{DS} = 40 - 6.725 \times 10^{-3}\,(3 \times 10^3 + 820) = 40 - 25.69 = 14.31 \text{ V}$$

$$V_{GS} = V_G - I_D\,R_S = 18 - 6.725 \times 10^{-3}\,(820) = 18 - 5.5145$$

$$= 12.4855 \text{ V}$$

3.13 Small Signal Model of D-MOSFET

Fig. shows as equivalent model of depletion type MOSFET.



(a) Symbol (b) AC equivalent model

This is exactly same as that of JFET. The only difference is that in depletion layer. MOSFET. V_{GSQ} can be positive for n-channel MOSFET and negative for p-channel MOSFET.

Due to this in depletion MOSFET, g_m can be greater than g_{mo}. This is illustrated in the following example.

3.14 Small Signal Model of E-MOSFET

We know that, in enhancement type MOSFET relationship between output current I_d and controlling voltage V_{GS} is given as,

$$I_d = K\,(V_{GS} - V_T)^2 \qquad \ldots (1)$$

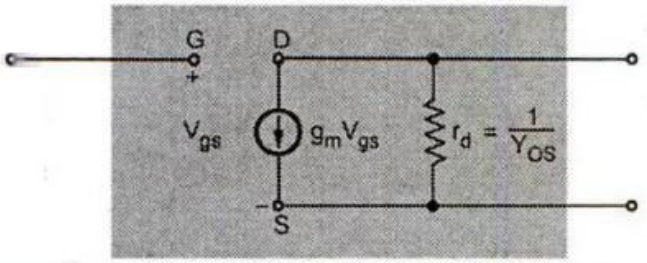


Fig_ ac equivalent model of enhancement type MOSFET

Fig. shows a.c. equivalent model of enhancement type MOSFET. This is exactly same as that of JFET. The only difference is that in enhancement type MOSFET, V_{GSQ} is positive for n channel MOSFET and negative for p-channel MOSFET.

where $$K = \frac{I_d\,(ON)}{(V_{GS}(ON) - V_T)^2}$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \qquad \ldots (2)$$

Thus, differentiating equation (2) with respect to V_{GS} we get the equation for g_m as follows,

$$g_m = \frac{I_D}{V_{GS}}$$

$$= V_{GS}\,[K\,(V_{GS} - V_T)]^2$$

$$= 2\,K\,(V_{GS} - V_T) \qquad \ldots (3)$$

3.15 Common Source amplifier using E-MOSFET

Figure 3.22. shows the circuit of a common source E-MOSFET amplifier. It is similar to a common emitter amplifier. Here the resistors R_1 and R_2 (called a voltage divider) are used to bias the field-effected transistor. The capacitor (C_1) and (C_2) are used to couple the a.c. input voltage source and the output voltage respectively, these are known as coupling capacitors. The capacitor (C_S) keeps the source of the MOSFET effectively at a.c. ground and is known as bypass capacitor.

The operation of the circuit may be understood from the assumption that when a small a.c. signal is applied to the gate, it produces variations in the gate-to-source voltage. This produces variations in the drain current.As the gate to source voltage

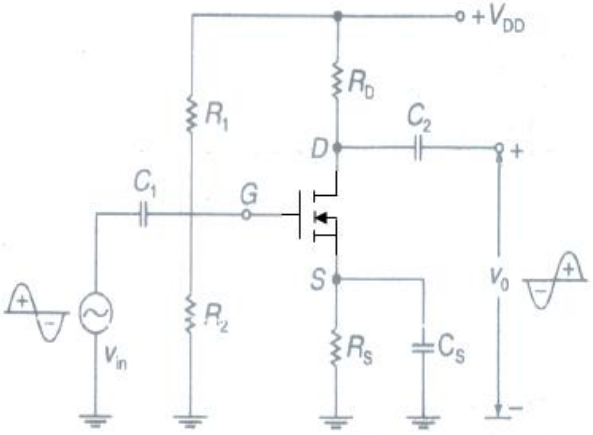


Fig. 3.22 Common Source Amplifier

increases, the drain current also increases. As a result of this, the voltage drop across the resistor (R_D) also increases. This causes the drain voltage to decrease. It means that the positive half cycle of the input voltage produces the negative half cycle of the output voltage. In other words, the output voltage (at the drain) is 180° out-of-phase with the input voltage (at the gate). This phenomenon of *phase inversion* is similar to that exhibited by a common emitter bipolar transistor amplifier.

3.15.1 Analysis of Common Source Amplifier

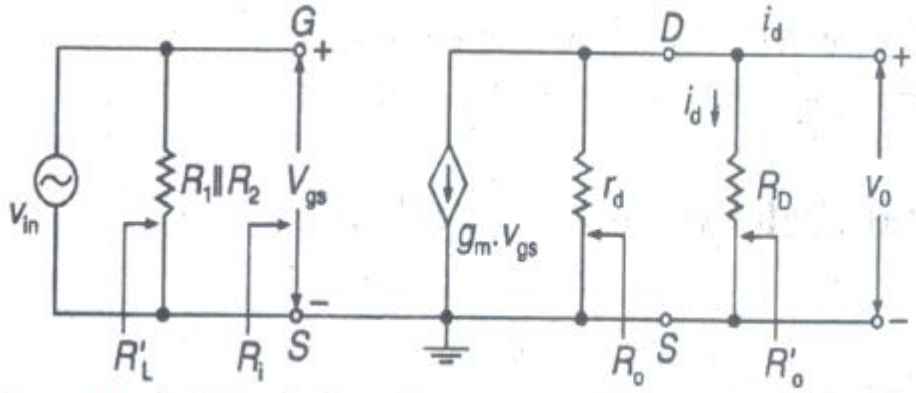


Fig. 3.23 A.C. equivalent circuit of a common source amplifier.

Figure 3.23 shows the a.c. equivalent circuit of a common source amplifier. This circuit has been obtained from the amplifier circuit shown in Figure 3.22 by short-circuiting the capacitors and the d.c. voltage supplies. The field-effect transistor is also replaced by its low-frequency model (or equivalent circuit). Now we shall use this circuit to find the expressions for amplifier voltage gain, *input resistance and output resistance.

1. *Voltage gain.* It is the ratio of the output voltage (v_o) to the input voltage (v_{in}). Mathematically the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

It may be noted that the current from the current source splits between the resistors r_d and R_D. The current through resistor R_D (as per current divider rule) is given by the relation,

$$i_d = \frac{r_d}{R_D + r_d} (g_m \cdot v_{gs})$$

and the output voltage,

$$v_o = - i_d \cdot R_D = - \left(\frac{r_d}{R_D + r_d} \right) (g_m \cdot v_{gs}) R_D$$

$$= -g_m \left(\frac{r_d \cdot R_D}{R_D + r_d} \right) v_{gs}$$

$$= -g_m (r_d \parallel R_D) \cdot v_{gs}$$

$$= -g_m \cdot r_L \cdot v_{gs} \quad \ldots (\because r_L = r_d \parallel R_D)$$

$$= -g_m \cdot r_L \cdot v_{in} \quad \ldots (\because v_{in} = v_{gs})$$

The minus sign indicates that the output voltage is 180° out-of-phase with the input voltage.

∴ Voltage

$$A_v = \frac{v_o}{v_{in}} = -g_m \cdot r_L$$

It may be noted that if the drain resistance (r_d) is sufficiently greater than resistor R_D, (*i.e.*, $r_d \geq 10\ R_D$) then the equivalent resistance of the resistors r_d and R_D in parallel,

$$r_L = R_D$$

and the voltage gain,

$$A_v = g_m \cdot R_D$$

Note. If the resistance R_D is much larger than r_d (*i.e.*, $R_D >> r_d$) then a.c. load resistance (r_L) is approximately equal to r_d.

2. *Input resistance.* It is the ratio of the input voltage (v_{in}) to the input current (i_{in}). Mathematically, the input resistance,

$$R_i = \frac{v_{in}}{i_{in}}$$

We know that input resistance (R_i) of a field-effect transistor is very high and hence can be considered to be infinity (*i.e.*, open-circuit). However, the input resistance of the amplifier stage (R'_i) is equal to the parallel combination of resistors R_1 and R_2 and the MOSFET input resistance (R_i). Thus

$$R'_i = (R_1 \parallel R_2) \parallel R_i$$

$$= R_1 \parallel R_2 \quad \ldots \text{(When } R_i \text{ is infinite)}$$

It may be noted that if we use a self-bias circuit (instead of a voltage divider bias), then the input resistance of the amplifier stage,

$$R'_i = R_G$$

3. *Output resistance.* It is the ratio of the output voltage (v_o) to the output current (i_d). Mathematically, the output resistance,

$$R'_o = \frac{v_o}{i_d}$$

We know that the output resistance (R_o) of a field-effect transistor is r_d. But for the amplifier stage, the output resistance is the parallel combination of resistors R_D and r_d. i.e.,

$$R'_o = R_D \| r_d$$

However, if $r_d >> R_D$, then the output resistance of amplifier stage,

$$R_o = R_D$$

By considering the Load Resistance (R_L)

$$r_L = R_D \| R_L$$

$$r_L = (R_D \| R_L) \| r_d$$

$$A_v = -g_m \cdot r_L$$

$$= -g_m (R_D \| R_L) \| r_d$$

$$= -g_m (R_D \| R_L) \quad \ldots (\text{If } r_d >> (R_D \| R_L))$$

and the output resistance, of the amplifier stage

$$R'_o = (R_D \| R_L) \| r_d$$

$$= R_D \| R_L \quad \ldots (\text{If } r_d >> (R_D \| R_L))$$

3.16 Common Drain Amplifier using E-MOSFET

Figure 3.24 shows the circuit of a common drain amplifier. It is similar to common collector (or emitter follower) amplifier. Self-biasing is used in the circuit. The input signal is applied to the gate through a coupling capacitor (C_1). And the output is taken from the source terminal through the coupling capacitor (C_2).

The operation of the amplifier may be understood by assuming that when a small a.c. signal is applied to the gate, it produces variations in the gate to source voltage.This

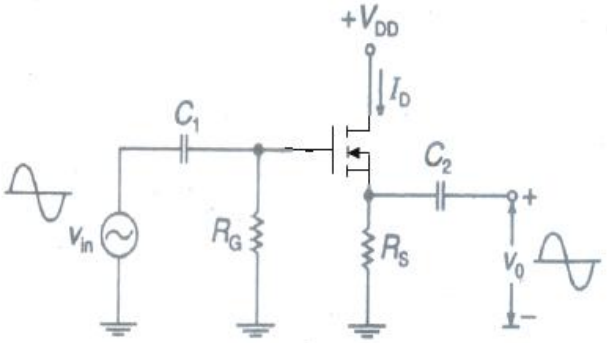


Fig. 3.24 Common Drain Amplifier

further produces the variations in drain current (I_D). As the gate-to-source voltage increases, the drain current also increases. As a result of this, the voltage drop across the source resistor (R_S) also increases. Thus the output voltage (v_o) increases. It may be noted that the output voltage of a common drain amplifier is approximately equal to and in phase with the input voltage. Because of this fact, the circuit is known as source follower.

A common drain amplifier (or a source follower) has a very high value of input resistance. It is because of this property that a common drain amplifier is used at the front end of measuring instruments like electronic voltmeters and cathode ray oscilloscopes.

3.16.1 Analysis of a Common Drain Amplifier

Figure 3.25 shows the a.c. equivalent circuit of a common drain amplifier. This circuit has been obtained from the amplifier circuit shown in Figure 3.24 by short circuiting the capacitors and d.c. voltage supply. The field-effect transistor is also replaced by its low-frequency model. Now we shall use this circuit to find the expressions for voltage gain, input resistance and output resistance.

1. *Voltage gain.* It is the ratio of output voltage (v_o) to the input voltage (v_{in}). Mathematically, the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

For the common drain amplifier, the input voltage,

$$v_{in} = v_{gs} + i_d \cdot R_s$$

and the output voltage,

$$v_o = i_d \cdot R_S$$

∴ Voltage gain,

$$A_v = \frac{v_o}{v_{in}} = \frac{i_d \cdot R_s}{v_{gs} + i_d \cdot R_s}$$

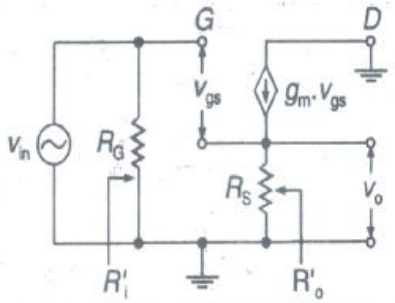


Fig. 3.25. A.C. equivalent circuit of a common drain amplifier.

Substituting the value of i_d ($= g_m \cdot v_{gs}$) in the above expression,

$$A_v = \frac{(g_m \cdot v_{gs})\, R_s}{v_{gs} + g_m \cdot v_{gs} \cdot R_s}$$

$$= \frac{g_m \cdot v_{gs} \cdot R_s}{v_{gs}\,(1 + g_m \cdot R_s)}$$

$$= \frac{g_m \cdot R_s}{1 + g_m \cdot R_s} = \frac{R_s}{R_s + \dfrac{1}{g_m}}$$

It may be noted that when R_s is much greater than $1/g_m$, the value of voltage gain approaches unity.

2. *Input resistance.* We know that the input signal is applied to the gate of the amplifier. As a result of this, the input resistance seen by the input signal source is extremely high just as in the common source configuration. The total input resistance (or the input resistance of the amplifier),

$$R'_i = R_G \parallel R_i$$

where R_i is the input resistance of the field effect transistor. Since the value of R_i is extremely high, therefore the total input resistance,

$$R'_i = R_G$$

3. *Output resistance.* We know that voltage gain of the common drain amplifier,

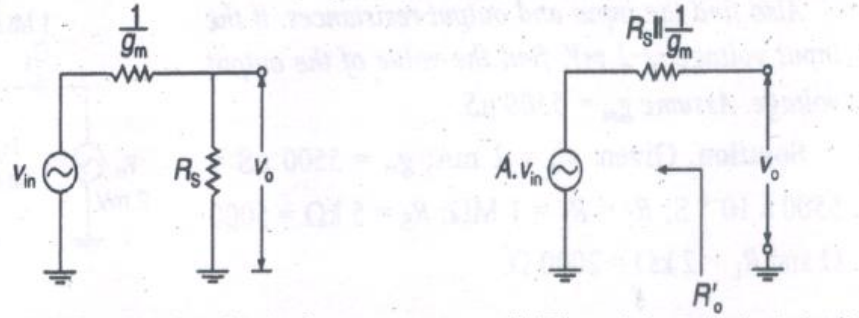
$$A_v = \frac{v_o}{v_{in}} = \frac{R_s}{R_s + \frac{1}{g_m}}$$

∴ Output voltage,

$$v_o = \left(\frac{R_s}{R_s + \frac{1}{g_m}} \right) \times v_{in}$$

The above expression is a voltage-divider equation. It implies that the input voltage (v_{in}) drives two resistors R_s and $1/g_m$ with output voltage taken across resistor (R_s). It means that the output side of the amplifier appears as shown in Figure 3.26 (*a*). It is evident from this figure, that the source resistor is driven by an a.c. source with an output resistance *i.e.*,

$$R_D = 1/g_m$$



(*a*) A.C. equivalent circuit of output side of the amplifier.

(*b*) Thevenin's equivalent circuit of the amplifier.

Fig. 3.26

It may be noted that output resistance (R_o) is the value of resistance looking back into the source terminal of the MOSFET . Now let us thevenize the output circuit. The resulting circuit is as shown in Figure 3.26 (*b*). It is evident from this figure, that the resistance R_s is in parallel with $1/g_m$ and the output resistance of the amplifier stage,

$$R'_o = R_s \parallel \frac{1}{g_m}$$

If the value of source resistance (R_s) is much larger than $1/g_m$, then the output resistance of the amplifier stage,

$$R'_o = \frac{1}{g_m}$$

3.17 Common Gate Amplifier using E-MOSFET

Figure 3.27 shows the circuit of a common gate amplifier. It is similar to a common base amplifier. The input signal is applied at the source through a coupling capacitor (C_1) and the output is taken from the drain through the coupling capacitor (C_2). The gate is effectively at a.c. ground because of the capacitor, (C_G).

The operation of the common gate amplifier may be understood from the assumption that when a small a.c. signal is applied to the source, it produces variation in gate-to-source voltage (V_{GS}). This inturn, produces the variations in drain current (I_D). As the gate-to-source voltage increases, the drain current also increases. As a result of this, the output voltage also increases. Thus output voltage of a common gate amplifier is in phase with the input voltage.

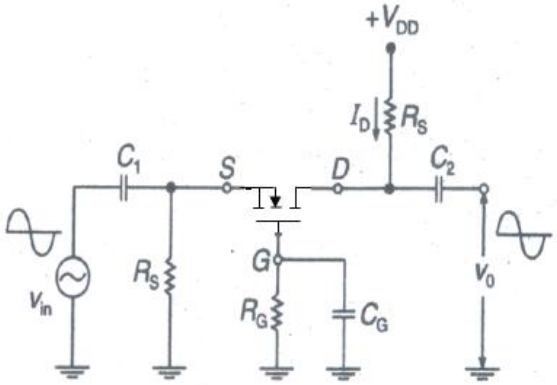


Fig. 3.27 Common gate amplifier.

A common gate amplifier has a low input resistance, high output resistance, high voltage gain and no phase reversal.

3.17.1 Analysis of a Common Gate Amplifier

Figure 3.28 shows an a.c. equivalent circuit of a common gate amplifier. This circuit has been obtained from the amplifier circuit shown in Figure 3.27 by short-circuiting the capacitors and the d.c. supply. The field-effect-transistor is also replaced by its low-frequency model.

Now we shall use this circuit to find the expressions for amplifier voltage gain, input resistance and output resistance.

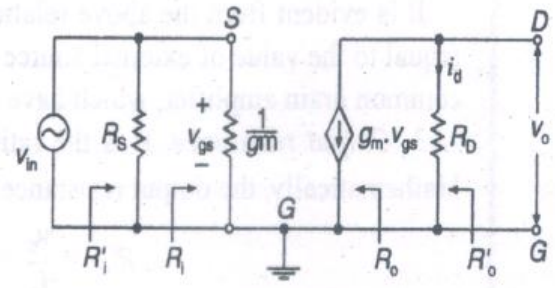


Fig. 3.28 Common gate amplifier.

1. *Voltage gain.* It is the ratio of a.c. output voltage (v_o) to the a.c. input voltage (v_{in}). Mathematically, the voltage gain,

$$A_v = \frac{v_o}{v_{in}}$$

We know that the a.c. input voltage,

$$v_{in} = v_{gs}$$

and the a.c. output voltage,

$$v_o = i_d \cdot R_D$$

$\therefore$ Voltage gain, $$A_v = \frac{i_d \cdot R_D}{v_{gs}}$$

Substituting the value of i_d (equal to $g_m \cdot v_{gs}$) in the above expression,

$$A_v = \frac{(g_m \cdot v_{gs}) \cdot R_D}{v_{gs}} = g_m \cdot R_D$$

It may be noted that the above expression for voltage gain is true only when there is no load resistor. If there is a load resistor (R_L) connected to the amplifier output, then the voltage gain.

$$A_v = g_m (R_D \parallel R_L)$$

2. *Input resistance.* It is the ratio of input voltage (v_{in}) to the input current (i_{in}). Mathematically, the input resistance,

$$R_i = \frac{v_{in}}{i_{in}}$$

For a common gate amplifier, the input voltage (v_{in}) is equal to the gate-to-source voltage (v_{gs}) and the input current (i_{in}) is equal to the drain current (i_d). Therefore the input resistance,

$$R_i = \frac{v_{gs}}{i_d} = \frac{v_{gs}}{g_m \cdot v_{gs}} \quad \ldots (\because i_d = g_m \cdot v_{gs})$$

$$= \frac{1}{g_m}$$

It may be noted that the resistance (R_i) is the value of input resistance looking directly into the source terminal of the JFET. The input resistance of the amplifier,

$$R'_i = R_s \parallel \frac{1}{g_m}$$

However, if R_s is much larger than the reciprocal of tranconductance ($1/g_m$) then the input resistance of the amplifier,

$$R'_i = R_s$$

It is evident from the above relation that a common gate amplifier has a low input resistance (equal to the value of external source resistance only). It is in contrast to the common source and common drain amplifier, which have extremely high input resistances.

3. *Output resistance.* It is the ratio of a.c. output voltage (v_o) to the a.c. output current (i_o). Mathematically, the output resistance of the amplifier,

$$R'_o = \frac{v_o}{i_o} = \frac{i_d \cdot R_D}{i_d} \qquad \ldots (\because v_o = i_d \cdot R_D \text{ and } i_o = i_d)$$
$$= R_D$$

It means that the output resistance of the common gate amplifier is equal to the external drain resistance (R_D). If there is a load resistor (R_L) connected to the amplifier output, then the output resistance of the amplifier,

$$R'_o = R_D \parallel R_L$$