BIASING OF FET AMPLIFIERS

Fixed Bias

Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum **transfer characteristics** make I_D levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents I_D and drain-source voltage V_{DS}, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for **JFET**s. Various FET biasing circuits are discussed below:
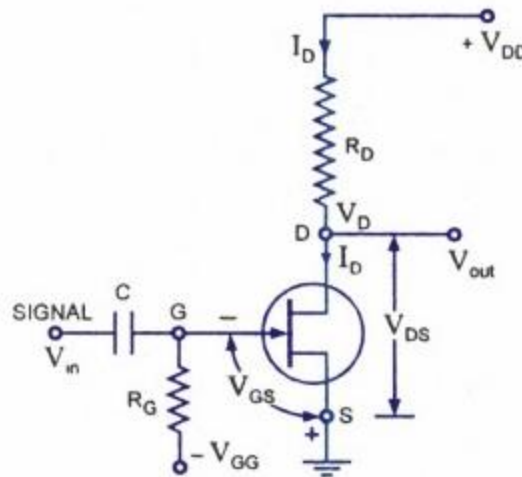
Fixed Bias:

FIG.: Fixed biasing circuit for JFET

DC bias of a FET device needs setting of gate-source voltage V_{GS} to give desired drain current I_D . For a JFET drain current is limited by the saturation current I_{DS}. Since the FET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET.

Fixed dc bias is obtained using a battery V_{QG}. This battery ensures that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal that is I_G =0. The battery provides a voltage V_{GS} to bias the N-channel JFET, but no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. While any ac signal will develop across R_G, the dc voltage drop across R_G is equal to $I_G R_G$ = 0 volt.

The gate-source voltage V_{GS} is then

$V_{GS} = - v_G - v_s = - v_{GG} - 0 = - V_{GG}$

The drain to source current I_D is then fixed by the gate-source voltage as determined by equation. This current then causes a voltage drop across the drain resistor R_D and is given as $V_{RD} = I_D R_D$ and output voltage, $V_{out} = V_{DD} - I_D R_D$
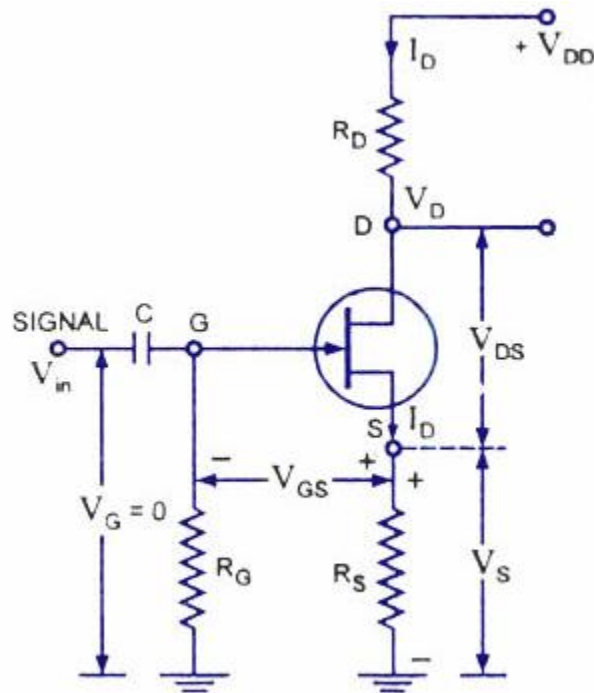
Self bias:

FIG.: Self bias circuit for JFET

This is the most common method for biasing a JFET. Self-bias circuit for N-channel JFET is shown in figure. Since no gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$ and, therefore,$v_G = i_G R_G = 0$ With a drain current I_D the voltage at the S is, $V_s = I_D R_s$. The gate-source voltage is then,

$V_{GS} = V_G - V_s = 0 - I_D R_s = - I_D R_s$ So, voltage drop across resistance R_s provides the biasing voltage V_{Gg} and no external source is required for biasing and this is the reason that it is called self-biasing. The operating point (that is zero signal I_D and V_{DS}) can easily be determined from equation and equation given below :

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

Thus dc conditions of JFET amplifier are fully specified. Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like transconductance. Let the given JFET be replaced by another JFET having the double conductance then drain current will also try to be double

but since any increase in voltage drop across R_s, therefore, gate-source voltage, V_{GS} becomes more negative and thus increase in drain current is reduced.

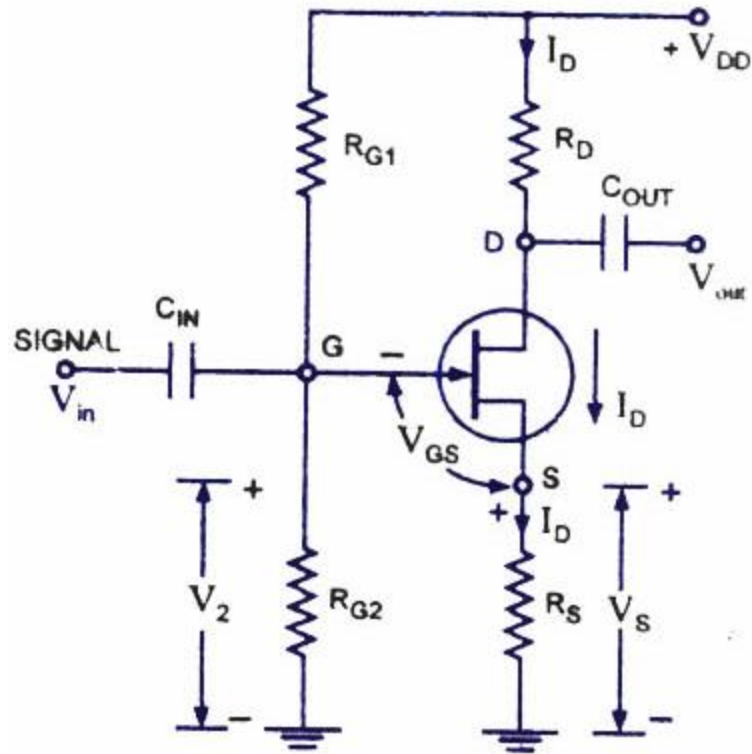**Potential Divider Bias for JFET:**

FIG.: Potential Divider Bias circuit for JFET

A slightly modified form of dc bias is provided by the circuit shown in figure. The resistors R_{G1} and R_{G2} form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias. The additional gate resistor R_{G1} from gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of larger valued R_s.

The gate is reverse biased so that $I_G = 0$ and gate voltage

$V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2}$

And

$V_{GS} = v_G - v_s = V_G - I_D R_s$

The circuit is so designed that $I_D R_s$ is greater than VG so that VGS is negative. This provides correct bias voltage.

The operating point can be determined as

$I_D = (V_2 - V_{GS})/ R_s$

And

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

FET SMALL SIGNAL ANALYSIS

Introduction:

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a current-controlled device and the FET is a voltage-controlled device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.

While the common-source configuration is the most popular, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.
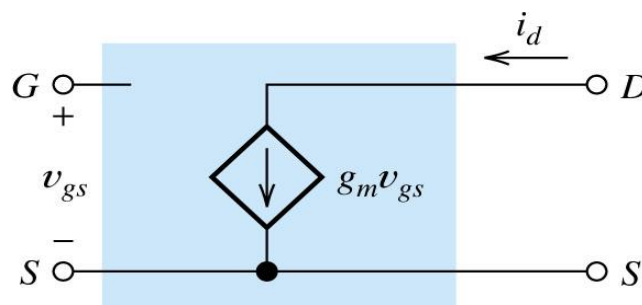
FIG.: Small signal model of FET

COMMON SOURCE AMPLIFIER

A common-source JFET amplifier is one in which the ac input signal is applied to the gate and the ac output signal is taken from the drain. The source terminal is common to both the input and output signal. A common-source amplifier either has no source resistor or has a bypassed source resistor, so the source is connected to ac ground. A self-biased common-source n-channel JFET amplifier with an ac source capacitively coupled to the gate is shown in Figure below. The resistor, RG, serves two purposes: It keeps the gate at approximately 0 V dc (because IGSS is extremely small), and its large value (usually several megohms) prevents loading of the ac signal source. A bias voltage is produced by the drop across RS. The bypass capacitor, C2, keeps the source of the JFET at ac ground.
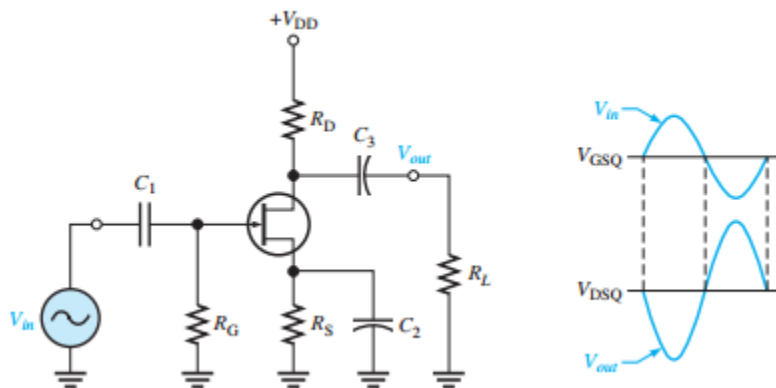

FIG.: Self biased Common source Amplifier

The input signal voltage causes the gate-to-source voltage to swing above and below its Q-point value (VGSQ), causing a corresponding swing in drain current. As the drain current increases, the voltage drop across RD also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in phase with the gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value (VDSQ) and is 180° out of phase with the gate-to-source voltage, as illustrated in Figure above. A Graphical Picture The operation just described for an n-channel JFET is illustrated graphically on both the transfer characteristic curve and the drain characteristic curve in Figure below. Part (a) shows how a sinusoidal variation, Vgs, produces a corresponding sinusoidal variation in Id. As Vgs swings from its Q-point value to a more negative value, Id decreases from its Q-point value. As Vgs swings to a less negative value, Id increases. The signal at the gate drives the drain

current above and below the Q-point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the ID axis and down to the VDS axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown. Because the transfer characteristic curve is nonlinear, the output will have some distortion. This can be minimized if the signal swings over a limited portion of the load line.
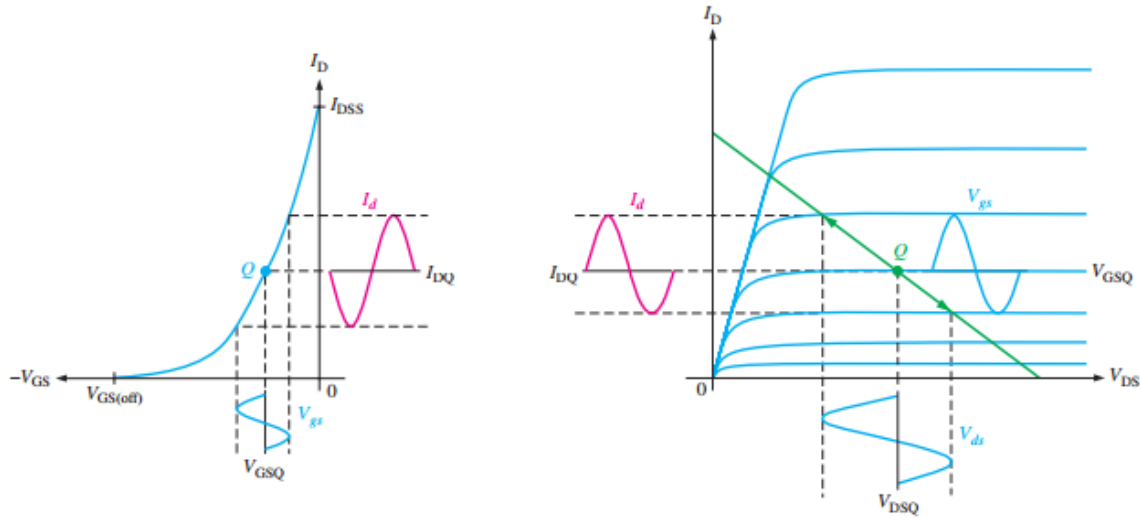

Fig. Transfer Characteristic curve and Drain curve for Common source JFET Amplifier

AC Equivalent Circuit to analyze the signal operation of the amplifier in Figure below ,an ac equivalent circuit is as follows. Replace the capacitors by effective shorts, based on the simplifying assumption that at the signal frequency. Replace the dc source by a ground, based on the assumption that the voltage source has a zero internal resistance. The VDD terminal is at a zero-volt ac potential and therefore acts as an ac ground. The ac equivalent circuit is shown in Figure below. Notice that the VDD end of Rd and the source terminal are both effectively at ac ground. Recall that in ac analysis, the ac ground and the actual circuit ground are treated as the same point.
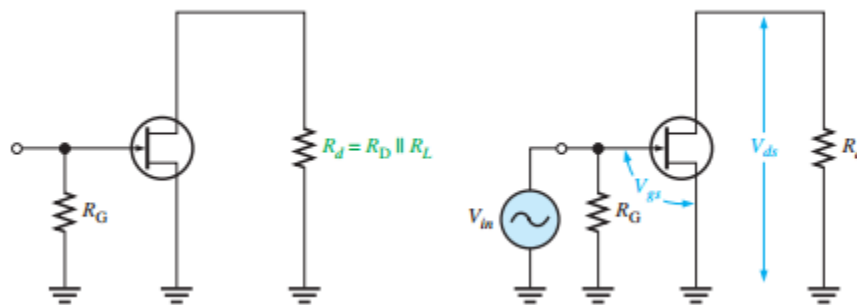

Fig: The AC equivalent circuit for Common source amplifier

An ac voltage source is shown connected to the input in Figure above. Since the input resistance to a JFET is extremely high, practically all of the input voltage from the signal source appears at the gate with very little voltage dropped across the internal source resistance. Vgs = Vin

$$V_{gs} = V_{in}$$

Voltage Gain The expression for JFET voltage gain that was given in Equation below applies to the common-source amplifier.

$$A_v = g_m R_d$$

Phase Inversion The output voltage (at the drain) is out of phase with the input voltage (at the gate). The phase inversion can be designated by a negative voltage gain, Recall that the common-emitter BJT amplifier also exhibited a phase inversion.

Input Resistance is derived as follows, because the input to a common-source amplifier is at the gate, the input resistance is extremely high. Ideally, it approaches infinity and can be neglected. As you know, the high input resistance is produced by the reverse-biased PN junction in a JFET and by the insulated gate structure in a MOSFET. The actual input resistance seen by the signal source is, the gate-to-ground resistor, RG, in parallel with the FET's input resistance, VGS IGSS. The reverse leakage current, IGSS, is typically given on the datasheet for a specific value of VGS so that the input resistance of the device can be calculated.

$$R_{in} = R_G \,||\, \left(\frac{V_{GS}}{I_{GSS}}\right)$$

Common drain JFET amplifier

A common-drain JFET amplifier is one in which the input signal is applied to the gate and the output is taken from the source, making the drain common to both. Because it is common, there is no need for a drain resistor. A common-drain JFET amplifier is shown in Figure below. A common-drain amplifier is also called a source-follower. Self-biasing is used in this particular circuit. The input signal is applied to the gate through a coupling capacitor, C1, and the output signal is coupled to the load resistor through C2.
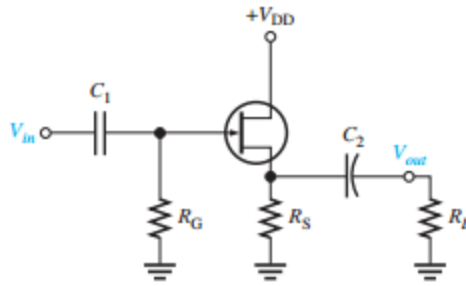
FIG.: Self biased Common Drain Amplifier

Voltage Gain as in all amplifiers, the voltage gain is Av Vout / Vin. For the source-follower, Vout is IdRs and Vin is Vgs IdRs as shown in above Figure. Therefore, the gate-to-source voltage gain is IdRs (Vgs IdRs). Substituting Id gmVgs into the expression gives the following result:

$$A_V = \frac{g_m v_{gs} R_s}{v_{gs} + g_m v_{gs} R_s}$$

The vgs term cancel so,

$$A_V = \frac{g_m R_s}{1 + g_m R_s}$$

Notice here that the gain is always slightly less than 1. If then a good approximation is Since the output voltage is at the source, it is in phase with the gate (input) voltage.

Input Resistance Because the input signal is applied to the gate, the input resistance seen by the input signal source is extremely high, just as in the common-source amplifier configuration. The gate resistor, RG, in parallel with the input resistance looking in at the gate is the total input resistance.

$$R_{in} = R_G \| R_{IN(gate)}$$

Where
$$R_{IN(gate)} = V_{GS} \| I_{GSS}$$

common gate amplifier

The common-gate FET amplifier configuration is comparable to the common-base BJT amplifier. Like the CB, the common-gate (CG) amplifier has a low input resistance. This is different from the CS and CD configurations, which have very high input resistances

Common-Gate Amplifier Operation A self-biased common-gate amplifier is shown in figure. The gate is connected directly to ground. The input signal is applied at the source terminal through C1. The output is coupled through C2 from the drain terminal.
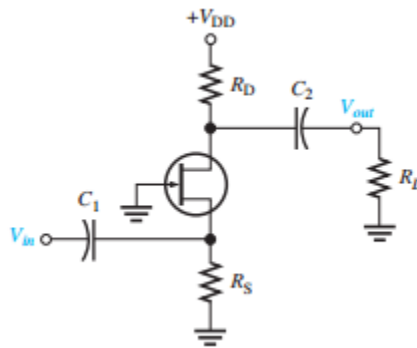

Fig: Common Gate Amplifier

Voltage Gain The voltage gain from source to drain is developed as follows:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_d}{V_{gs}} = \frac{I_d\,R_d}{V_{gs}} = \frac{g_m\,V_{gs}\,R_d}{V_{gs}}$$

$$A_v = g_m R_d$$

Where Rd = RD || RL. Notice that the gain expression is the same as for the common-source JFET amplifier.

Input Resistance As you have seen, both the common-source and common-drain configurations have extremely high input resistances because the gate is the input terminal. In contrast, the common-gate configuration where the source is the input terminal has a low input resistance. This is shown as follows. First, the input current is equal to the drain current

$$I_{in} = I_s = I_d = g_m V_{gs}$$

Second, the input voltage equals Vgs.

$$V_{in} = V_{gs}$$

Therefore, the input resistance at the source terminal is

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{gs}}{g_m V_{gs}}$$

$$R_{in} = \frac{1}{g_m}$$

MOSFET BIASING:

Biasing of Enhancement MOSFET:

Drain to Gate bias**:**

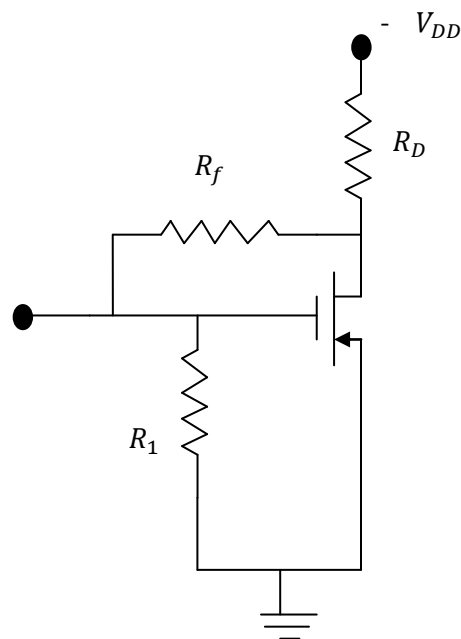The following figure shows the drain to gate bias circuit for enhancement mode MOSFET.

FIG. : Drain to Gate bias circuit for enhancement MOSFET.

Here, the bias voltage is $v_{GS} = \left[\frac{R_1}{R_1 + R_f}\right] V_{DS}$.

This circuit offers the DC stabilization through the feedback resistor R_f. However, the input resistance is reduced because of Miller effect. Also, the voltage divider biasing technique given for JFET can be used for the enhancement MOSFET. Here, the DC stability is accomplished by the DC feedback through R_s.

But the self- bias technique given for JFET cannot be used for establishing an operating point for the enhancement MOSFET because the voltage drop across R_s is in a direction to reverse-bias the gate and it actually needs forward gate bias.

Potential Divider Bias:

The following figure shows the circuit diagram. The MOSFET is a N- channel enhancement mode MOSFET common source circuit with source resistor.
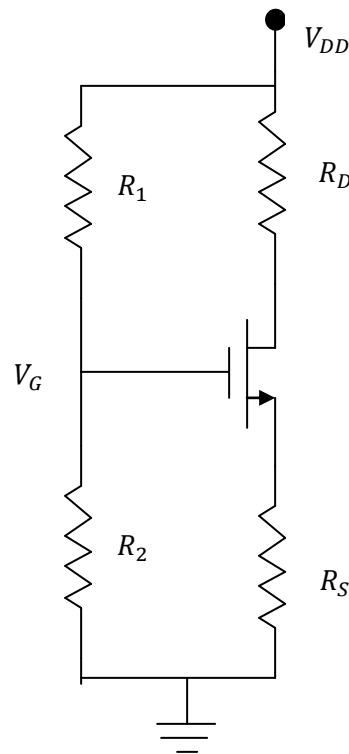

FIG.: N-Channel enhancement mode MOSFET common source circuit with source resistor.

The gate voltage is

$$V_G = V_{GS} = \left[\frac{R_1}{R_1 + R_2}\right] V_{DD}$$

And the gate to source voltage is

$$V_{GS} = V_{DD} - V_G$$

Assuming that $V_{GS} > V_{TN}$ and the MOSFET is biased in the saturation region, the drain current is

$$I_D = K_N (V_{GS} - V_{TN})^2$$

Here the threshold voltage V_{TN} and conduction parameter K_N are functions of temperature.

The drain to source voltage is $V_{DS} = V_{DD} - I_D R_D$

If $V_{DS} > V_{DS} (sat) = V_{GS} > V_{TN}$, then the MOSFET is biased in the saturation region. If

$V_{DS} < V_{DS} (sat) = V_{GS} > V_{TN}$, then the MOSFET is biased in the non -saturation region and the drain current is given by,

$$I_D = K_N (2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2$$

Biasing of depletion MOSFET:

Both the self bias and voltage divider bias circuit given for JFET can be used to establish an operating point for the depletion mode MOSFET.

Small signal analysis of MOSFET:

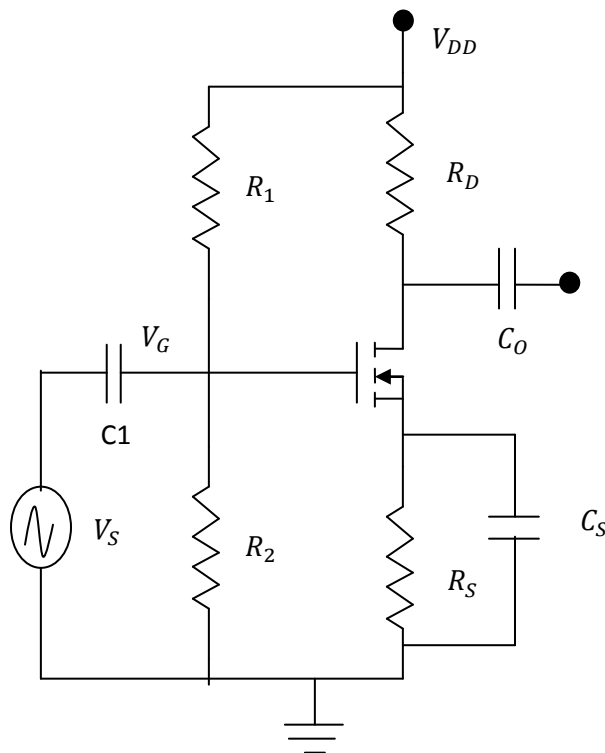**Common source configuration of E- MOSFET with potential divider biasing:**

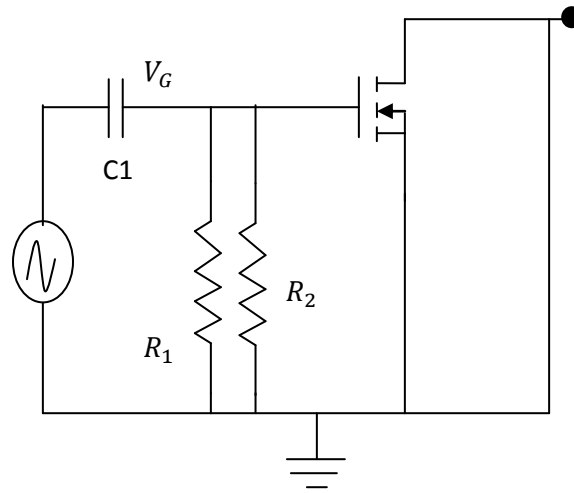FIG.: Circuit Diagram of common source amplifier

FIG.: AC Equivalent circuit

In common source configuration of E-MOSFET, the inputs is fed to the gate and output is taken at the drain. The resistor R1 and R2 acts as biasing resistors. For AC analysis the source is connected to ground and hence source terminal is connected to both input and output.

The circuit diagram of voltage-divider bias for E-MOSFET is shown in the above figure. The AC equivalent model of the voltage –divider bias circuit of E-MOSFET can be obtained by shorting the capacitors and grounding the biasing sources as shown in the above figure. Replacing the devices by its small signal model, We get the figure shown below.
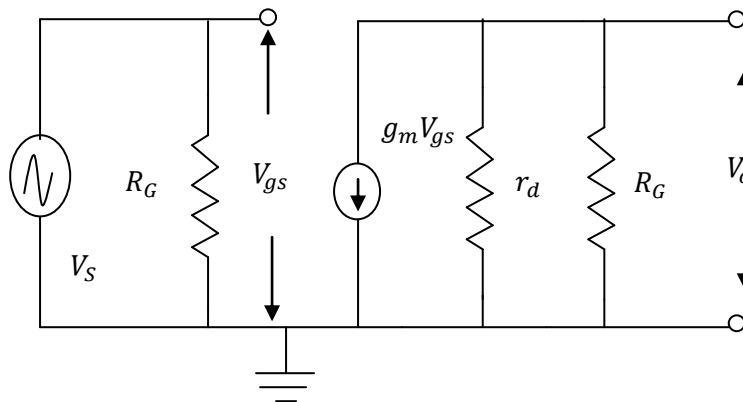
FIG.: Small signal equivalent circuit for common source amplifier

Input impedance:

      Input impedance is the resistance looking back from the input terminal. From the small signal signal model of voltage divider configuration of E-MOSFET shown in the above figure, the input impedance can be calculated as

$$Z_i = R_1 || R_2$$

Output impedance:

      Output impedance is the resistance looking back from the output terminal. From the small signal; model of MOSFET, The output impedance is calculated as follows,

$$Z_o = R_D || r_d$$

When Vi = 0, gate- source voltage, V_{gs} = 0 . Therefore, $g_m V_{gs}$ is an open circuit. Hence the output impedance is equal to drain resistance. Therefore, the output impedance is given by,

$$Z_o = R_D$$

Voltage gain:

Voltage gain is the ratio of output voltage to input voltage.

$$A_V = \frac{V_o}{V_i}$$

$$V_o = I_O(R_D || r_d) = I_D(R_D || r_d)$$

Where, $I_D = g_m V_{gs}$

Therefore, $A_V = \frac{V_o}{V_i} = - g_m R_D$

Common Drain Amplifier:

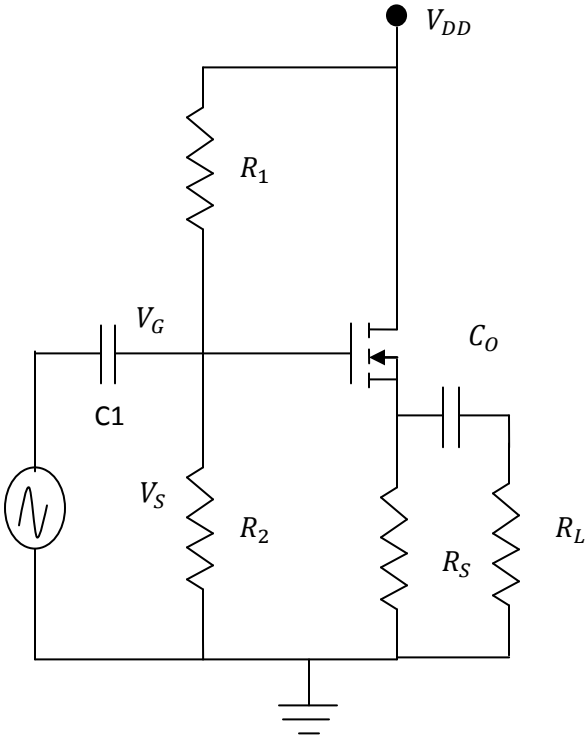The circuit diagram and the small signal diagram are as follows

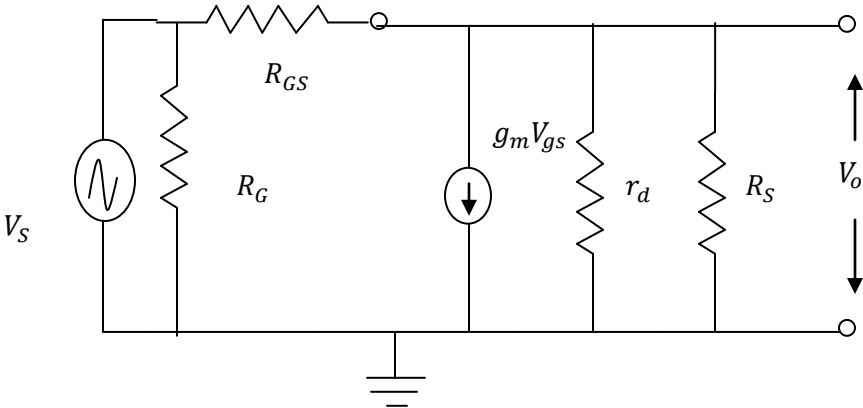FIG.: Circuit Diagram of common drain Amplifier

FIG.: Small signal model of common drain amplifier

Input Impedance is given by, $Z_g = R_{GS}[1 + g_m(R_S || R_L)]$;

Therefore,

$$Z_i = R_G || Z_g$$

The output impedance is

$$Z_O = R_S || (1/g_m)$$

Voltage Gain is,

$$A_v = 1$$

Common Gate Amplifier:

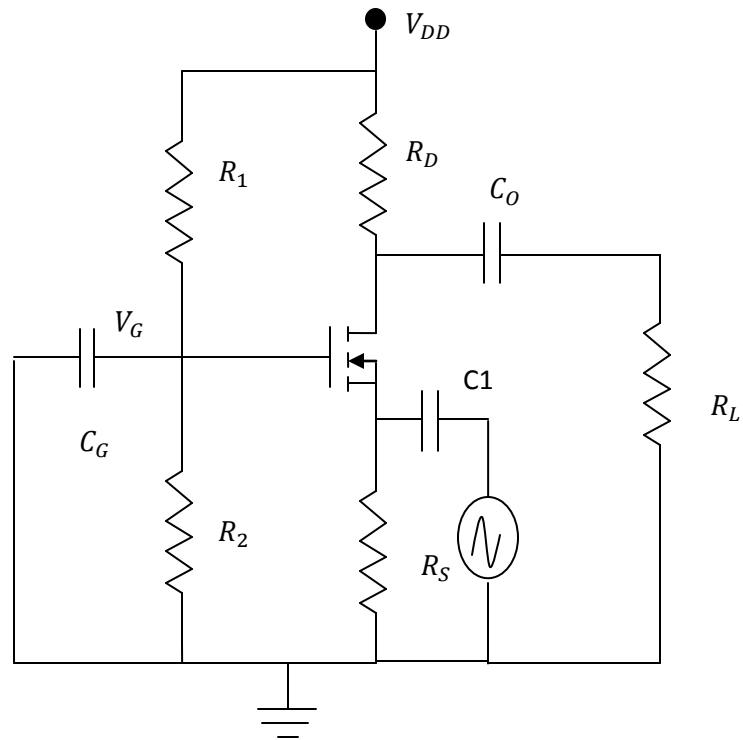The circuit diagram and the small signal model are given below
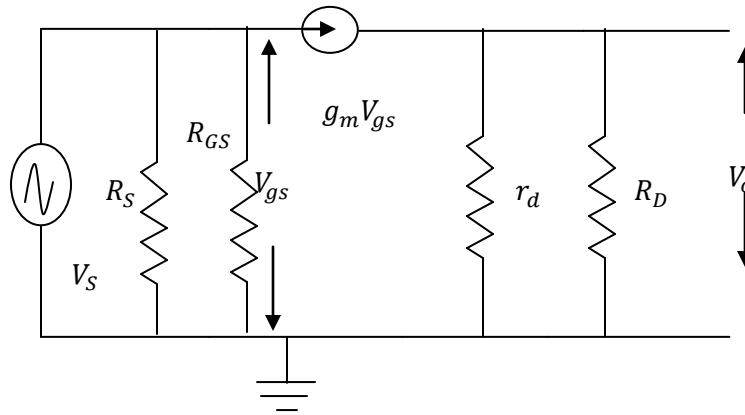

FIG.: Common gate amplifier

FIG.: Small signal model of common gate amplifier

Input Impedance, $\qquad$ $Z_i = R_S || 1/g_m$

Output Impedance, $\qquad$ $Z_O = R_D || r_d$

Voltage Gain, $\qquad$ $A_V = \frac{V_o}{V_i} = g_m(R_D || r_d || R_L)$