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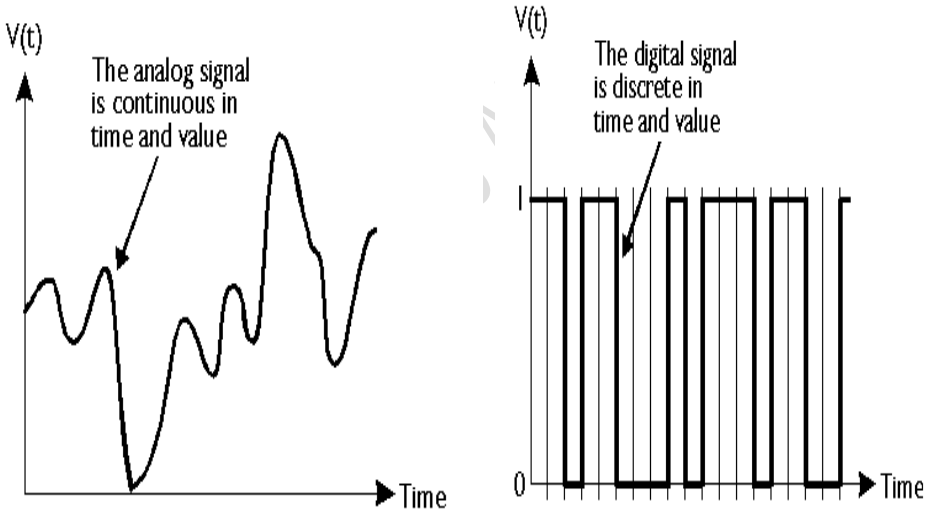
UNIT :5

Introduction to ADC / DAC - Specifications, ADC Quantization Error, Types of ADC - Flash, Counter, Successive Approximation, Dual-Slope types and Introduction to Delta-Sigma, Types of DAC - Weighted-Resistor, 2R ladder and PWM type, ADC and DAC Problems - Smart sensors.

ANALOG TO DIGITAL CONVERTOR

Definition:

An electronic integrated circuit which converts a signal from analog (continuous and can take an inifinity of values) to digital (discrete digital data) form. Provides a link between the analog world of transducers and the digital world of signal processing and data handling.

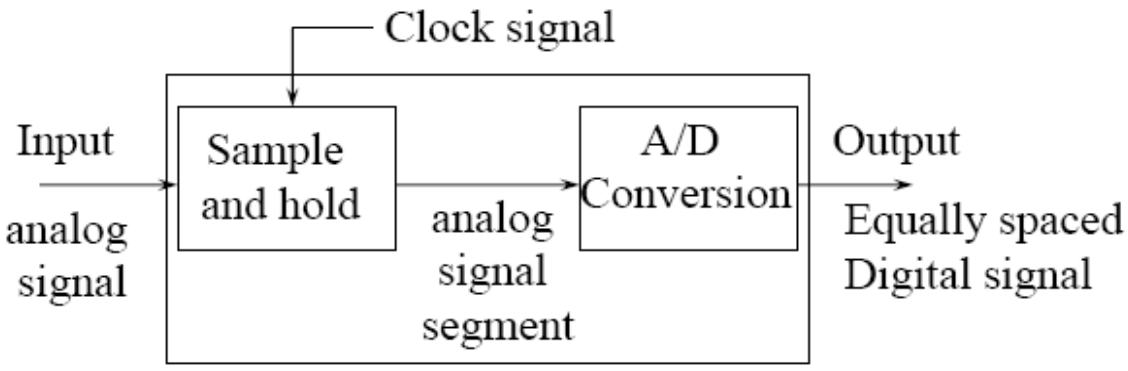


Examples of A/D Applications

1. Microphones - Take your voice varying pressure waves in the air and convert them into varying electrical signals
2. Strain Gages - Determines the amount of strain (change in dimensions) when a stress is applied
3. Thermocouple – Temperature measuring device converts thermal energy to electric energy
4. Voltmeters

5. Digital Multimeters

Basic circuit:



Process of Analog to Digital Conversion:

1. Sampling and Holding
2. Quantizing - Breaking down analog value in to a set of finite states
3. Encoding - Assigning a digital word or number to each state and matching it to the input signal

Sampling and Holding

The circuit is an analog device that **samples** the voltage of a continuously varying analog signal and **holds** (freezes) its value at a constant level for a specified minimum period of time.

- Measuring analog signals at uniform time intervals
  - Ideally twice as fast as what we are sampling
- Digital system works with discrete states
  - Taking samples from each location
- The signal is only defined at determined times
- The sampling times are proportional to the sampling period ($\mathbf{T_s}$)

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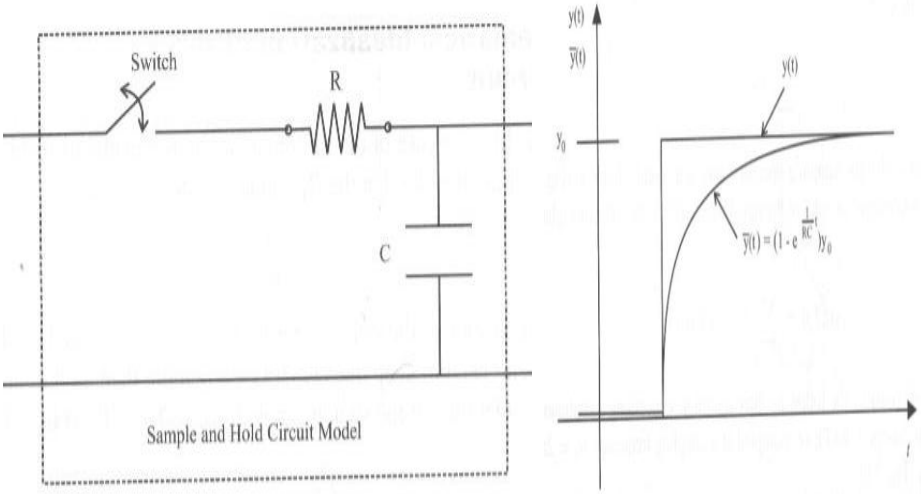

Respose of sample and Hold Circuit

- Switch ON – sampling of signal (time to charge capacitor w/ V_{in})
- Switch OFF - voltage stored in capacitor (hold operation)
- Must hold sampled value constant for digital conversion

Aliasing

- High and low frequency samples are indistinguishable
- Occurs when the input signal is changing much faster than the sample rate.
- Results in improper conversion of the input signal
- For example, a 2 kHz sine wave being sampled at 1.5 kHz would be reconstructed as a 500 Hz (the aliased signal) sine wave.
- Usually exists when Nyquist Criterion is violated
- Prevented through the use of Low-Pass (Anti-aliasing) Filters

Nyquist Rule:

Use a sampling frequency at least twice as high as the maximum frequency in the signal to avoid aliasing.

$\mathbf{f_s > 2 * f_{max}}$

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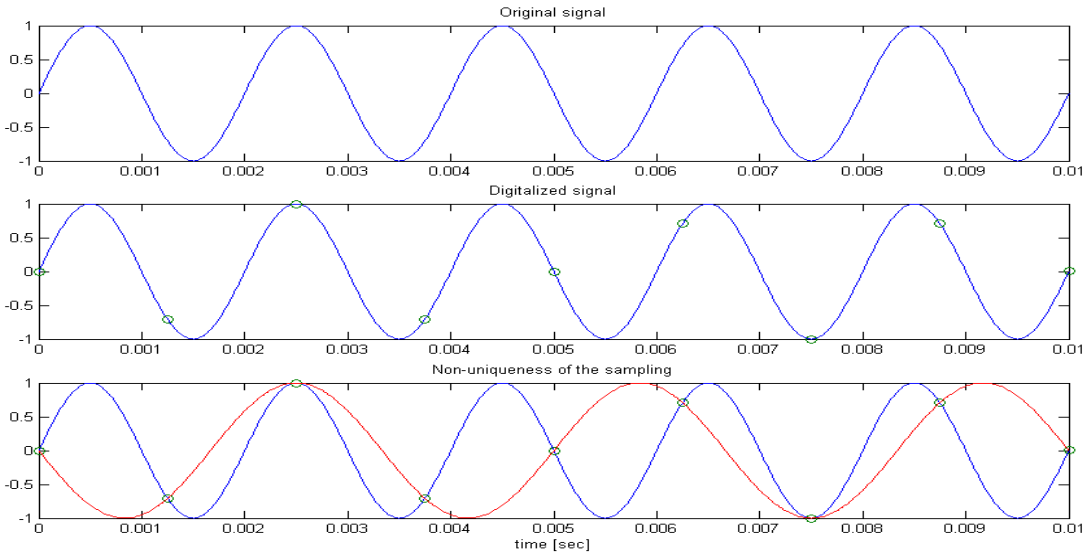

Quantizing and Encoding

- Approximates a continuous range of values and replaces it with a binary number
- Error is introduced between input voltage and output binary representation
- Error depends on the resolution of the ADC.
- Separating the input signal into a discrete states with K increments

$$K=2^N$$

N is the number of bits of the ADC

Analog quantization size

$$Q =(V_{max}-V_{min})/2^N$$

Q is the Resolution

(or)

$$Q= \Delta V_r/N$$

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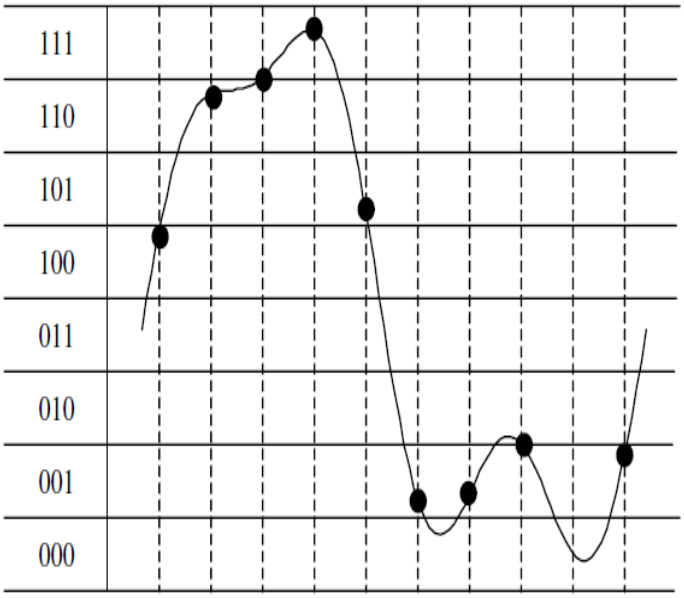
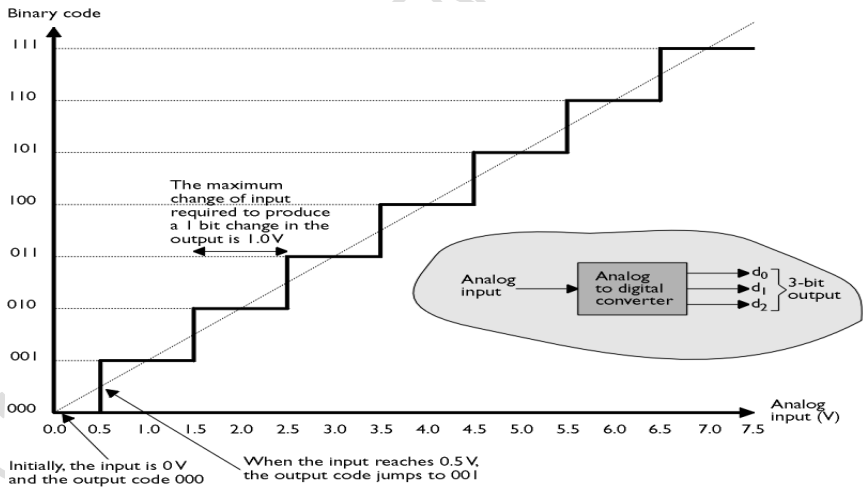


Resolution

- Maximum value of quantization error
- Error is reduced with more available memory

V_{range}=Input Voltage Range

n= # bits of ADC



Example:

$$resolution = V_{range}/(2^n - 1)$$

$V_{range} = 7.0V$

$n = 3$

$1V = 7V/(2^3 - 1)$

1V-Resolution

- Resolution (number of discrete values the converter can produce) = Analog Quantization size (Q).
- limited by signal-to-noise ratio (should be around 6dB)

Accuracy of A/D Conversion

There are two ways to best improve accuracy of A/D conversion:

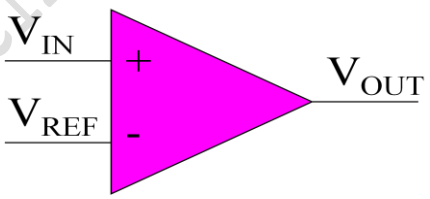
- Increasing the resolution (Q) which improves the accuracy in measuring the amplitude of the analog signal.
- Increasing the sampling rate (T_s) which increases the maximum frequency that can be measured

A/D Converter Types:

1. Flash ADC
2. Delta-Sigma ADC
3. Successive Approximation ADC
4. Dual Slope (integrating) ADC

Flash ADC

- Consists of a series of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which produces a binary output
- **Working**
- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs



- If $V_{IN} > V_{REF}$:Output is High
- If $V_{IN} < V_{REF}$:Output is Low

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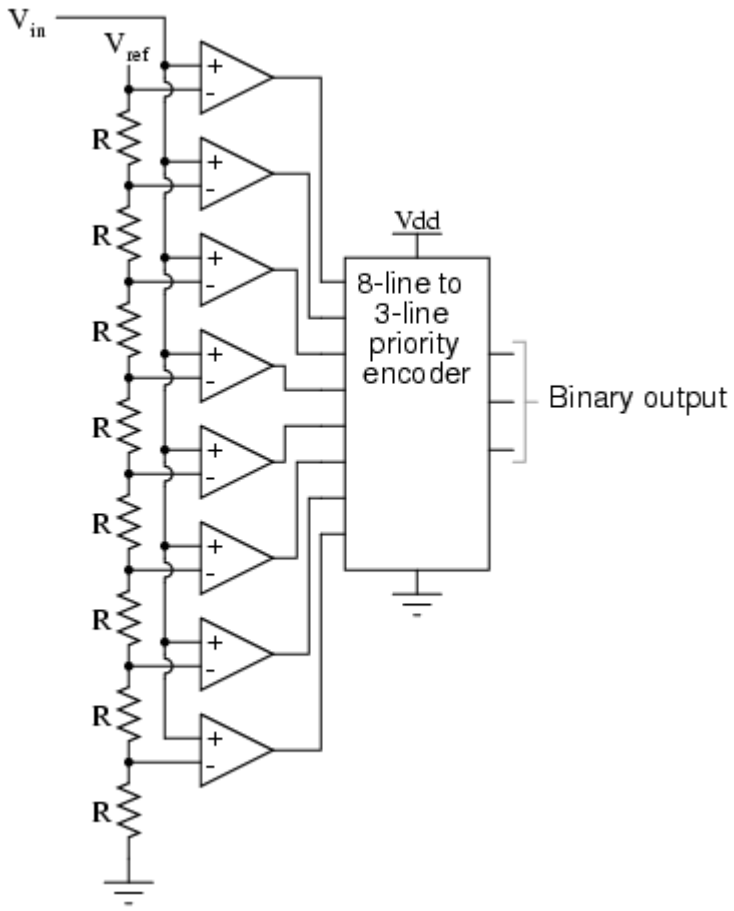
Flash ADC Circuit



Example:

V_{in} = 5.5V, V_{ref}= 8V

V_{in} lies in between V_{comp5} & V_{comp6}

$V_{comp5} = V_{ref}*5/8 = 5V$

$V_{comp6} = V_{ref}*6/8 = 6V$

Comparator 1 - 5 => output **1**

Comparator 6 - 7 => output **0**

Encoder Octal Input = sum(0011111) = 5

Encoder Binary Output = 1 0 1

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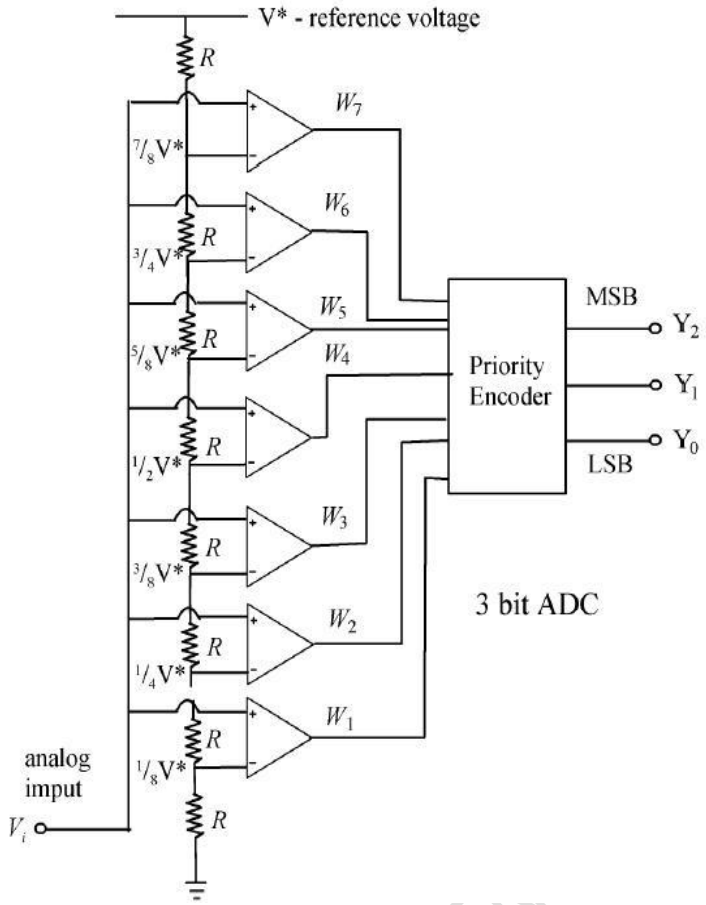


Advantages

- Simplest in terms of operational theory
- Most efficient in terms of speed, very fast
- limited only in terms of comparator and gate propagation delays

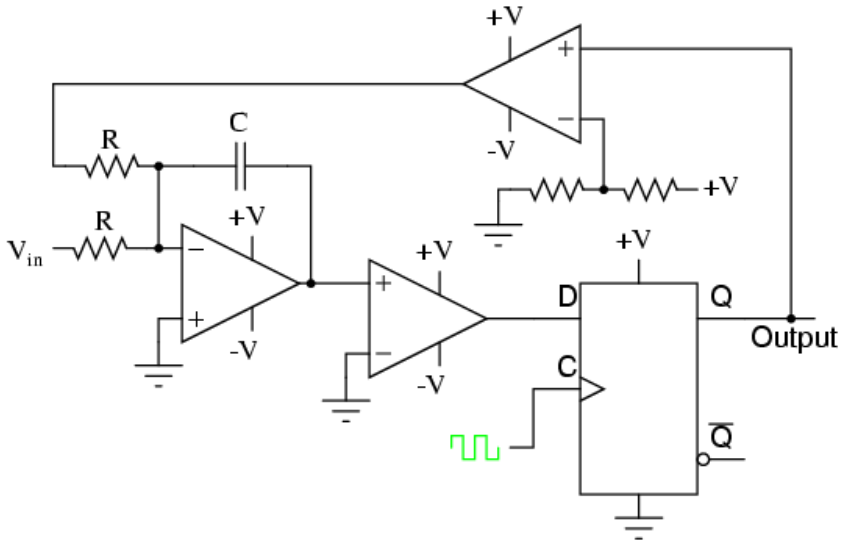
Disadvantages

- Lower resolution
- Expensive
- Large Power Consumption
- For each additional output bit, the number of comparators is doubled
    - i.e. for 8 bits, 256 comparators needed

Sigma Delta ADC

- Over sampled input signal goes to the integrator
- Output of integration is compared to GND

- Iterates to produce a serial bit stream
- Output is serial bit stream with # of 1's proportional to V_{in}



Advantages

- High resolution
- No precision external components needed

Disadvantages

Slow due to oversampling

Successive Approximation ADC

- A Successive Approximation Register (SAR) is added to the circuit
- Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the MSB and finishing at the LSB.
- The register monitors the comparators output to see if the binary count is greater or less than the analog signal input and adjusts the bits accordingly

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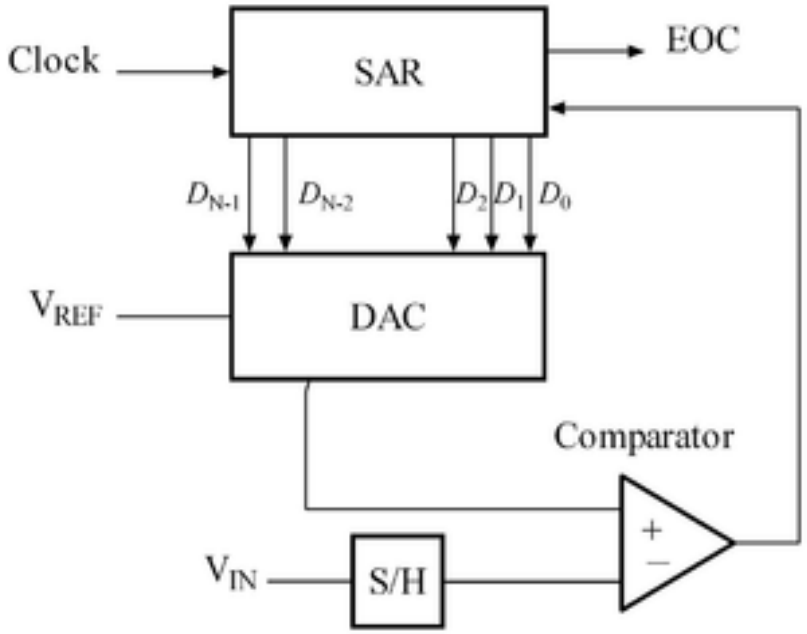
Successive Approximation ADC Circuit



Elements:

- DAC = Digital to Analog Converter
- EOC = End of Conversion
- SAR = Successive Approximation Register
- S/H = Sample and Hold Circuit
- V_{in} = Input Voltage
- Comparator
- V_{ref} = Reference Voltage

Algorithm

- Uses an n-bit DAC and original analog results
- Performs a binary comparison of V_{DAC} and V_{in}
- MSB is initialized at 1 for DAC
- If $V_{in} < V_{DAC}$ ($V_{REF} / 2^{\wedge n=1}$) then MSB is reset to 0
- If $V_{in} > V_{DAC}$ ($V_{REF} / 2^{\wedge n}$) Successive Bits set to 1 otherwise 0
- Algorithm is repeated up to LSB
- At end DAC in = ADC out

- N-bit conversion requires N comparison cycles

Example 1:

5-bit ADC, V_{in}=0.6V, V_{ref}=1V

Cycle 1 => MSB=1

SAR = 1 0 0 0 0

$V_{DAC} = V_{ref}/2^{\wedge 1} = .5$ $V_{in} > V_{DAC}$ SAR unchanged = 1 0 0 0 0

- Cycle 2

SAR = 1 1 0 0 0

V_{DAC} = .5 +.25 = .75 $V_{in} < V_{DAC}$ SAR bit3 reset to 0 = 1 0 0 0 0

- Cycle 3

SAR = 1 0 1 0 0

V_{DAC} = .5 + .125 = .625 $V_{in} < V_{DAC}$ SAR bit2 reset to 0 = 1 0 0 0 0

- Cycle 4

SAR = 1 0 0 1 0

V_{DAC} = .5+.0625=.5625 $V_{in} > V_{DAC}$ SAR unchanged = 1 0 0 1 0

- Cycle 5

SAR = 1 0 0 1 1

V_{DAC} = .5+.0625+.03125= .59375

Bit	4	3	2	1	0
Voltage	.5	.25	.125	.0625	.03125

Advantages

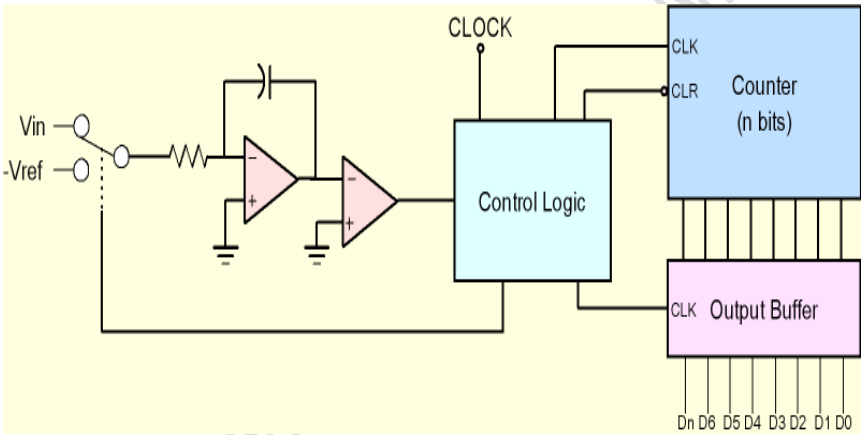
- Capable of high speed and reliable
- Medium accuracy compared to other ADC types
- Good tradeoff between speed and cost
- Capable of output the binary number in serial (one bit at a time) format.
- High resolution
- No precision external components needed

Disadvantages

- Higher resolution successive approximation ADC's will be slower
- Speed limited to ~5Msps

Dual Slope ADC

- An unknown input voltage is applied to the input of the integrator and allowed to ramp for a fixed time period (t_u)
- Then, a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (t_d)
- The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period
- The run-down time measurement is usually made in units of the converter's clock, so <u>longer integration times allow for higher resolutions</u>
- The speed of the converter can be improved by sacrificing resolution



$$V_{in} = -V_{ref} \frac{t_d}{t_u}$$

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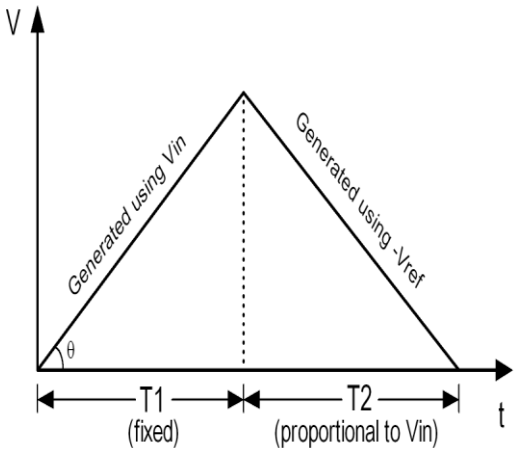


$$\left(V(t) = V(0) + \frac{V_{in}\,t}{RC}\right)^{*}$$

Comparison

Type	Speed (relative)	Cost (relative)
Dual Slope	Slow	Med
Flash	Very Fast	High
Successive Appox	Medium – Fast	Low
Sigma-Delta	Slow	Low

INTRODUCTION TO DELTA-SIGMA:

Delta-sigma (**ΔΣ**; or **sigma-delta**, **ΣΔ**) modulation is a method for encoding analog signals into digital signals as found in an analog-to-digital converter (ADC). It is also used to transfer high bit-count low frequency digital signals into lower bit-count higher frequency digital signals as part of the process to convert digital signals into analog as part of adigital-to-analog converter (DAC).

In a conventional ADC, an analog signal is integrated, or sampled, with a sampling frequency and subsequently quantized in a multi-level quantizer into a digital signal. This process introduces quantization error noise. The first step in a delta-sigma

modulation is delta modulation. In delta modulation the change in the signal (its delta) is encoded, rather than the absolute value. The result is a stream of pulses, as opposed to a stream of numbers as is the case with PCM. In delta-sigma modulation, the accuracy of the modulation is improved by passing the digital output through a 1-bit DAC and adding (sigma) the resulting analog signal to the input signal, thereby reducing the error introduced by the delta-modulation.

Primarily because of its cost efficiency and reduced circuit complexity, this technique has found increasing use in modern electronic components such as DACs, ADCs, frequency synthesizers, switched-mode power supplies and motor controllers.

Both ADCs and DACs can employ delta-sigma modulation. A delta-sigma ADC first encodes an analog signal using high-frequency delta-sigma modulation, and then applies a digital filter to form a higher-resolution but lower sample-frequency digital output. On the other hand, a delta-sigma DAC encodes a high-resolution digital input signal into a lower-resolution but higher sample-frequency signal that is mapped to voltages, and then smoothed with an analog filter. In both cases, the temporary use of a lower-resolution signal simplifies circuit design and improves efficiency.

In brief, because it is very easy to regenerate pulses at the receiver into the ideal form transmitted. The only part of the transmitted waveform required at the receiver is the time at which the pulse occurred. Given the timing information the transmitted waveform can be reconstructed electronically with great precision. In contrast, without conversion to a pulse stream but simply transmitting the analog signal directly, all noise in the system is added to the analog signal, permanently reducing its quality.

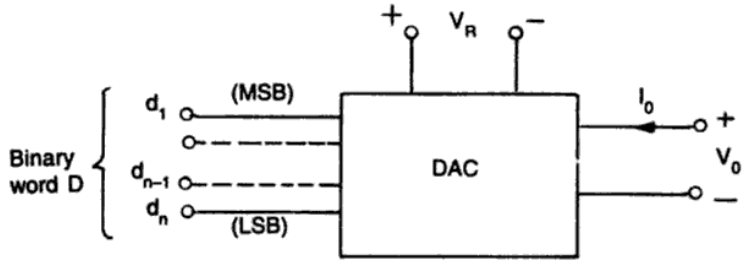
Each pulse is made up of a step up followed after a short interval by a step down. It is possible, even in the presence of electronic noise, to recover the timing of these steps and from that regenerate the transmitted pulse stream almost noiselessly. Then the accuracy of the transmission process reduces to the accuracy with which the transmitted pulse stream represents the input waveform.

Delta-sigma modulation converts the analog voltage into a pulse frequency and is alternatively known as Pulse Density modulation or Pulse Frequency modulation. In general, frequency may vary smoothly in infinitesimal steps, as may voltage, and both

may serve as an analog of an infinitesimally varying physical variable such as acoustic pressure, light intensity, etc. The substitution of frequency for voltage is thus entirely natural and carries in its train the transmission advantages of a pulse stream. The different names for the modulation method are the result of pulse frequency modulation by different electronic implementations, which all produce similar transmitted waveforms.

The ADC converts the mean of an analog voltage into the mean of an analog pulse frequency and counts the pulses in a known interval so that the pulse count divided by the interval gives an accurate digital representation of the mean analog voltage during the interval. This interval can be chosen to give any desired resolution or accuracy. The method is cheaply produced by modern methods; and it is widely used.

5.1 DIGITAL TO ANALOG CONVERTER:



The input in the digital to analog converter is an n-bit binary word D and is combined with a reference voltage V_r to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K\ V_{FS}\ (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \quad \cdot (1)$$

Where,

V_o = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1\ d_2 \ldots\ldots d_n$ = n-bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = most significant bit (MSB) with a weight of V_{FS}/2^n

There are various ways of implementing DAC

- Weighted-Resistor DAC
- 2R ladder DAC
- PWM type DAC

5.1.1 WEIGHTED RESISTOR DAC

One of the simplest circuits is shown in Fig. 5.1.1(a) uses a summing amplifier with a binary weighted resistor network. It has n- electronic switches $d_1\ d_2 \ldots\ldots d_n$ controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage (-V_R). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 5.1.1(a), the output current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \quad \text{----- (2)}$$

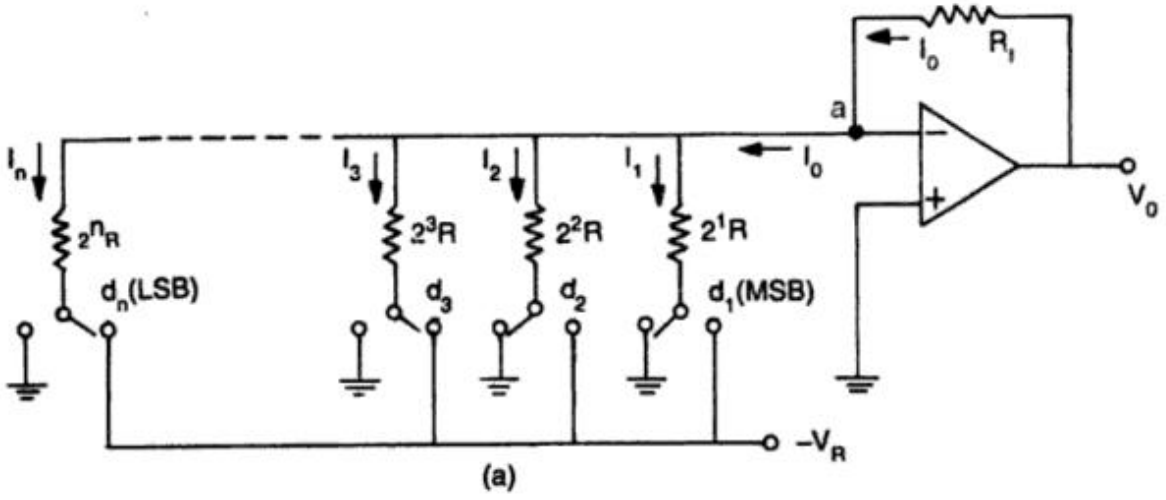
Comparing equation (1) with (2) it can be seen that if R_f = R then K = 1 and V_{FS}= V_R .

The circuit shown in Fig. 5.1.1(a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 5.1.1(b) for a 3-bit weighted resistor DAC. It may be noted that

- ✓ Although the op-amp in Fig. 5.1.1(a) is connected in inverting mode, it can also be connected in non-inverting mode.
- ✓ The op-amp is simply working as a current to voltage converter.

- ✓ The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be = 5 V and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are 2^0R, 2^1 R, 2^2 R… 2^7 R. the largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5 kΩ. The fabrication of such a large resistance is IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as 2.5 kΩ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.



(a)

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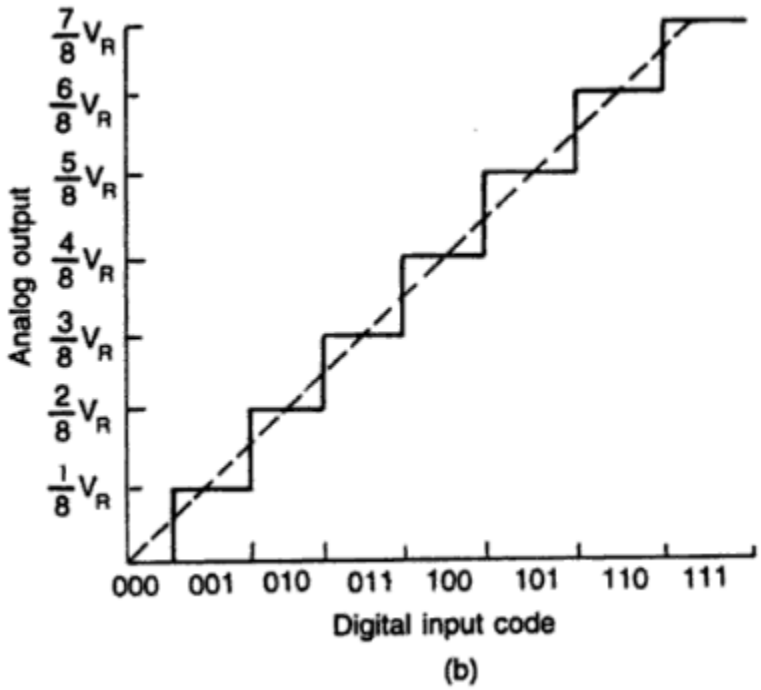

Fig. 5.1.1(a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

5.1.2 R-2R ladder type DAC:

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of resistor ranges from 2.5kΩ to 10kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 5.1.2(a), where the switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 5.1.2(b) and finally to Fig. 5.1.2(c). then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

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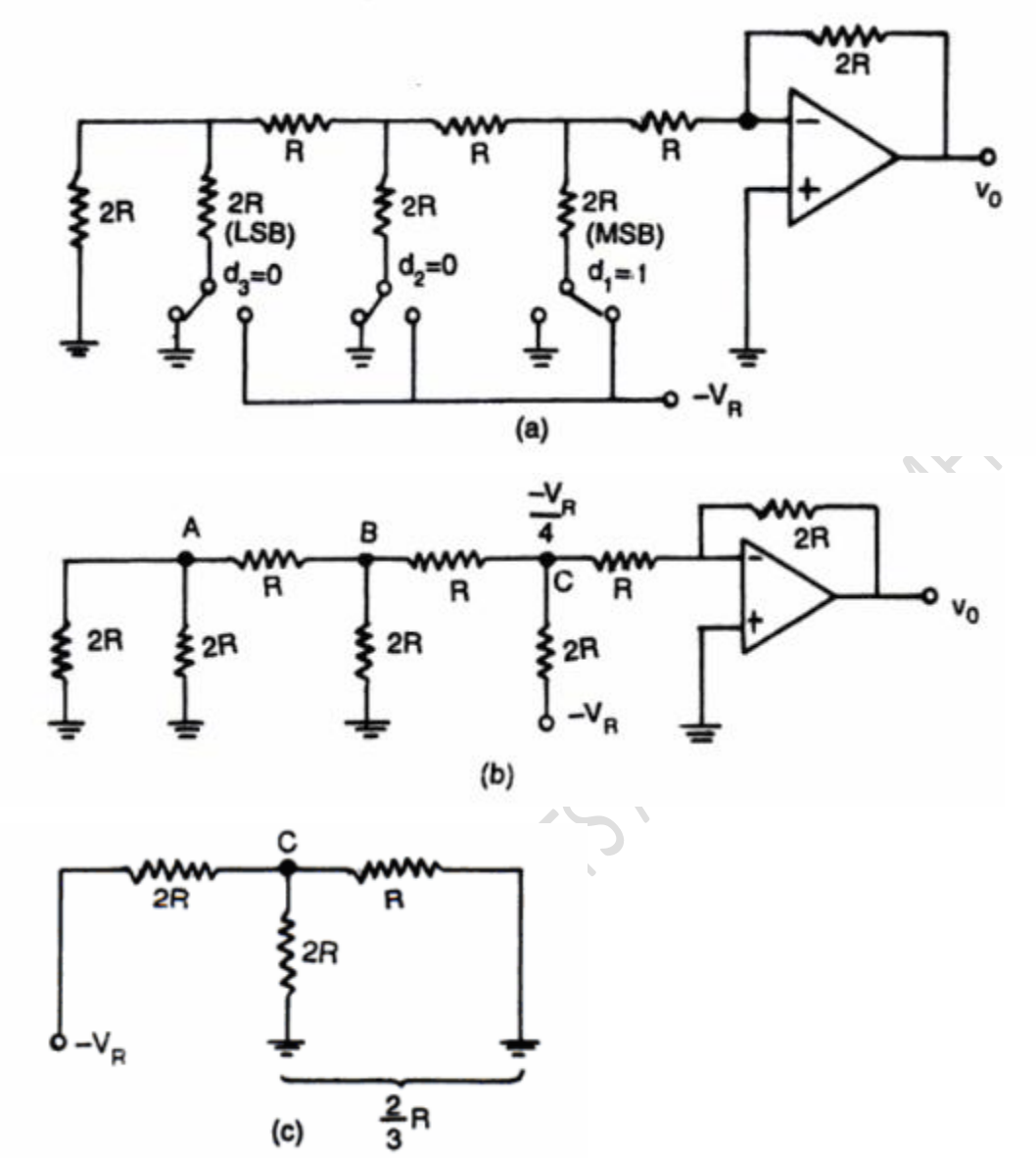


Fig. 5.1.2(a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The output voltage

$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 5.1.3(a). The circuit can be simplified to the equivalent form of Fig. 5.1.3(b). The

voltages at the nodes (A,B,C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_0 = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

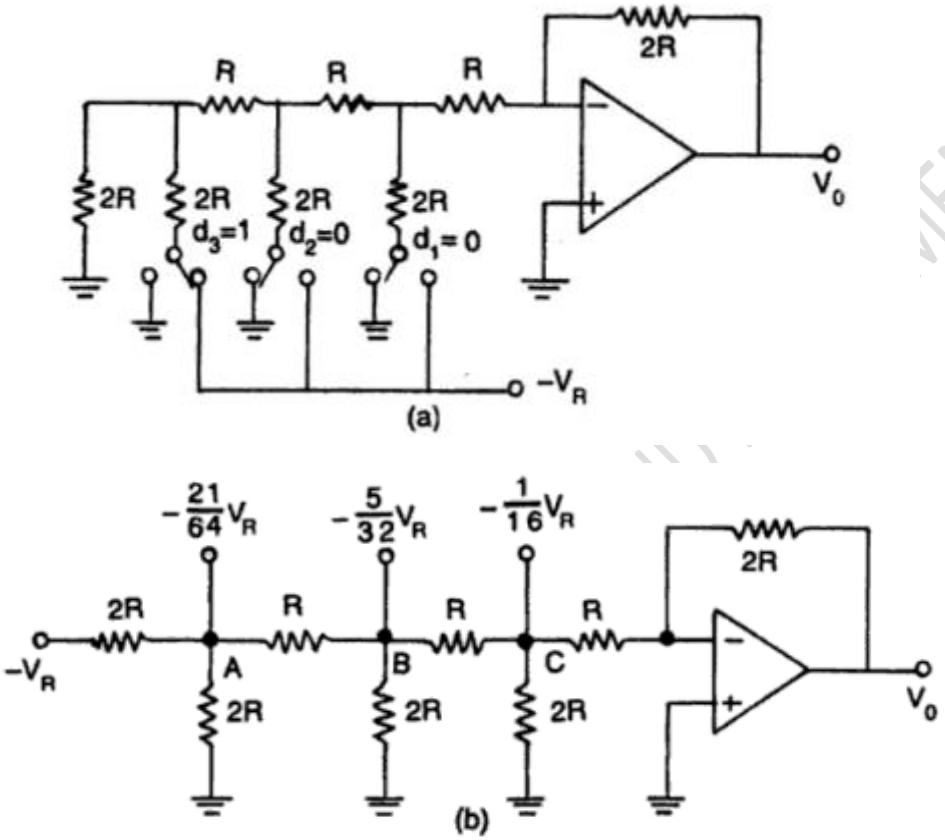


Fig. 5.1.3(a) R-2R ladder DAC for switch positons 001 (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

5.1.3 PWM TYPE DAC

The PWM signal outputs on a device are variable duty cycle square-waves with 3.3 volt amplitude. These signals can each be decomposed into a D.C. component plus a new square-wave of identical duty-cycle but with a time-average amplitude of zero. Figure below depicts this graphically.

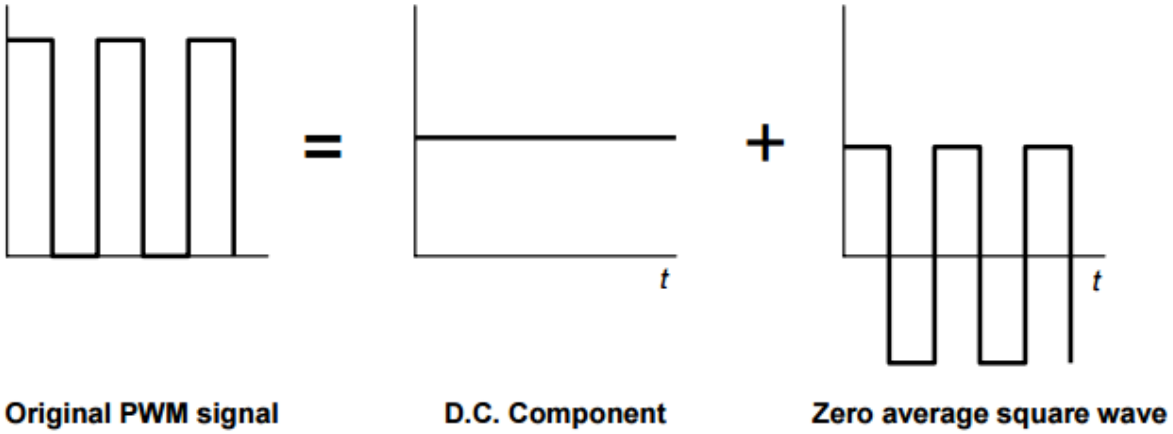


Fig. 5.1.4 Decomposition of PWM signal

The idea behind realizing digital-to-analog (D/A) output from a PWM signal is to analog low-pass filter the PWM output to remove most of the high frequency components, ideally leaving only the D.C. component. This is depicted in Figure below Fig. 5.1.5. The bandwidth of the low-pass filter will essentially determine the bandwidth of the digital-to-analog converter. A frequency analysis of the PWM signal is given in the next section in order to provide a theoretical basis for the filtering strategy.

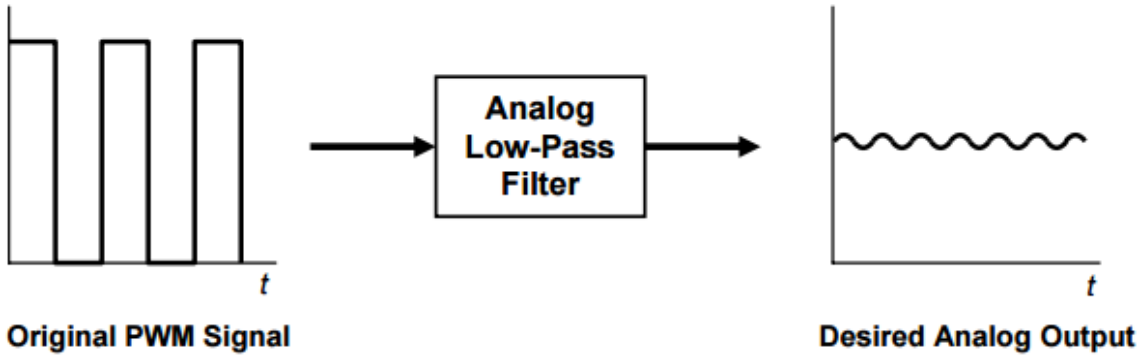


Fig. 5.1.5 analog filtering of PWM signal

The PWM/DAC approach is not new, but performance limitations have historically confined its use to low-resolution, low-bandwidth applications. The performance of the method relates directly to the ability of the low-pass filter to remove the high-frequency components of the PWM signal. Use a filter with too low a cut-off frequency, and DAC

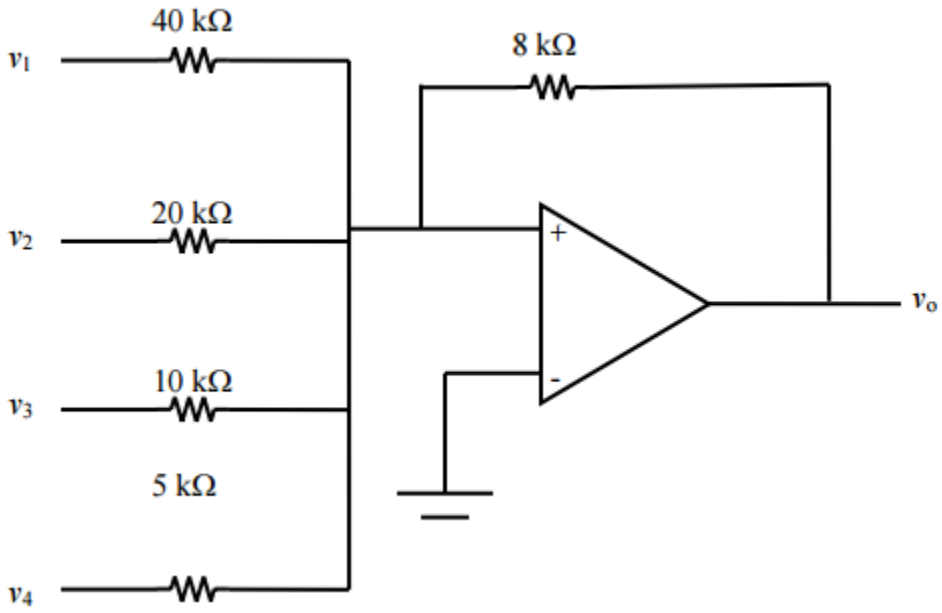
bandwidth suffers. Use a filter with too high a cut-off frequency or with slow stop-band rolloff, and DAC resolution suffers. These issues will be discussed in more detail later in this report, but one way to alleviate both of these problems is to increase the frequency of the PWM. However, as PWM frequency increases on conventional microprocessor generated PWM, digital resolution problems begin to manifest. It will be seen in this report that the hi-resolution PWM module (HRPWM) on the device of digital signal controllers is able to overcome these performance limitations to a great extent and offer real-world useable DAC performance.

PROBLEMS ON ADC AND DAC

1. Design a digital-to-analog (DAC) that produces an analog output voltage vo equal -1 V times the 4-bit number at the input.

   Solution

   The bits (least significant to most significant) are represented by v1, v2, v3, and v4. Logic 1 is represented by 5 V and logic 0 by 0 V. One possible design is shown in the following Figure.



V_4	V_3	V_2	V_1	V_o
0	0	0	0	0
0	0	0	5	-1
0	0	5	0	-2
0	0	5	5	-3
0	5	0	0	-4
0	5	0	5	-5
0	5	5	0	-6
0	5	5	5	-7
5	0	0	0	-8
5	0	0	5	-9
5	0	5	0	10
5	0	5	5	-11
5	5	0	0	-12
5	5	0	5	-13
5	5	5	0	-14
5	5	5	5	-15

In summation, each input receives a different gain or weighting

$$v_o = -1.6v_4 - 0.8v_3 - 0.4v_2 - 0.2v_1$$

5.1.4 SMART SENSORS

A **smart transducer** is an analog or digital transducer or actuator combined with a processing unit and a communication interface.

As sensors and actuators become more complex they provide support for various modes of operation and interfacing. Some applications require additionally fault-tolerance and distributed computing. Such high-level functionality can be achieved by adding an embedded microcontroller to the classical sensor/actuator, which increases the ability to cope with complexity at a fair price.

In the machine vision field, a single compact unit which combines the imaging functions and the complete image processing functions is often called a smart sensor.

They are often made using CMOS, VLSI technology and may contain MEMS devices leading to lower cost. They may provide full digital outputs for easier interface or they may provide quasi-digital outputs like pulse width modulation.

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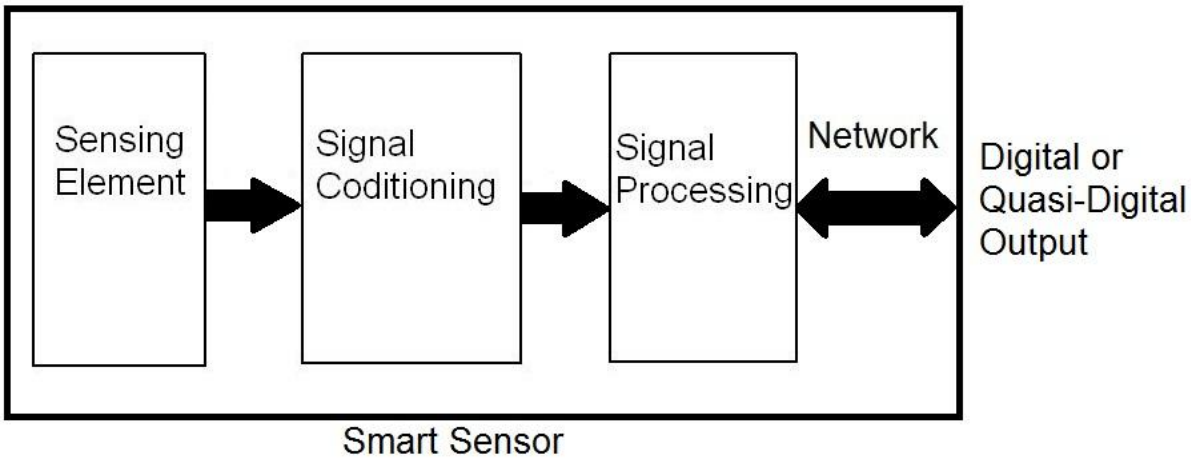

Advantages

1. Compact
2. Higher reliability
3. Lower cost
4. Can be done using existing cmos processes
5. Ease of use
6. electronic data storage
7. self-indication
8. auto correction
9. auto display