UNIT – II

TRANSISTOR BIASING CIRCUITS ANS SMALL SIGNAL ANALYSIS OF BJT AMPLIFIERS 9 Hrs.

Biasing- Types of biasing- DC equivalent circuit of BJT- Load Line-DC and AC Load Line Analysis – Hybrid Model of BJT- Hybrid Model Analysis of CE, CB, CC - Calculation of Input Impedance, Output Impedance, Voltage Gain, Current Gain using hybrid model- Approximate Model of BJT- CE, CB and CC Analysis- Small signal equivalent circuit of BJT- Small Signal Analysis of CE, CB and CC.

Biasing

For proper working of a transistor, it is essential to apply external voltages of correct polarity across its emitter-base and collector-base junctions.

- emitter-base junction is always forward biased
- collector-base junction is always reverse-biased
  This type of biasing is known as *FR* biasing

Stability Factor

The degree of success achieved in stabilizing I_C in the face of variations in I_{CO} is expressed in terms of current stability factor S. It is defined as the rate of change of I_C with respect to I_{CO} when both β and I_B (V_{BE}) are held constant.

$$\therefore \qquad S = \frac{dI_C}{dI_{CO}} \qquad \text{— } \beta \text{ and } I_B \text{ constant}$$

Larger the value of S, greater the thermal instability and ***vice versa*** (in view of the above, this factor should, more appropriately, be called instability factor !).

The stability factor may be alternatively expressed by using the well-known equation $I_C = I\beta + (I + \beta) I_{CO}$ which, on differentiation with respect to I_C, yields.

$$I = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_{CO}}{dI_C} = \beta \frac{dI_B}{dI_C} + (1+\beta)\frac{1}{S} \qquad \therefore \qquad S = \frac{(1+\beta)}{1-\beta(dI_B / dI_C)}$$

The stability factor of any circuit can be found by using the general formula

$$S = \frac{1 + R_B / R_E}{1 + (1-\alpha)\ (R_B / R_E)}$$

where R_B = ***total*** series parallel resistance in the base

R_E = ***total*** series dc resistance in the emitter

α = dc alpha of the transistor

Different Methods for Transistor Biasing

Some of the methods used for providing bias for a transistor are :

1. Base Bias or Fixed Current Bias

It is not a very satisfactory method because bias voltages and currents do not remain constant during transistor operation.

2. Base Bias with Emitter Feedback

This circuit achieves good stability of dc operating point against changes in β with the help of emitter resistor which causes degeneration to take place.

3. Base Bias with Collector Feedback

It is also known as collector-to-base bias or collector feedback bias. It provides better bias stability.

4. Base Bias with Collector And Emitter Feedbacks

It is a combination of (2) and (3) above.

5. Emitter Bias with Two Supplies

This circuit uses both a positive and a negative supply voltage. Here, base is at approximately 0 volt *i.e.* $V_B \cong 0$.

6. Voltage Divider Bias

It is most widely used in linear discrete circuits because it provides good bias stability. It is also called universal bias circuit or base bias with one supply.

Base Bias with Emitter Feedback

1. At saturation, V_{CE} is essentially zero, hence V_{CC} is distributed over R_L and R_E.

$$\therefore \qquad I_{C(sat)} = \frac{V_{CC}}{R_E + R_L}$$

2. I_C can be found as follows :

Consider the supply, base, emitter and ground route. Applying Kirchhoff 's Voltage Law, we have

$$-I_B R_B - V_{BE} - I_E R_E + V_{CC} = 0$$

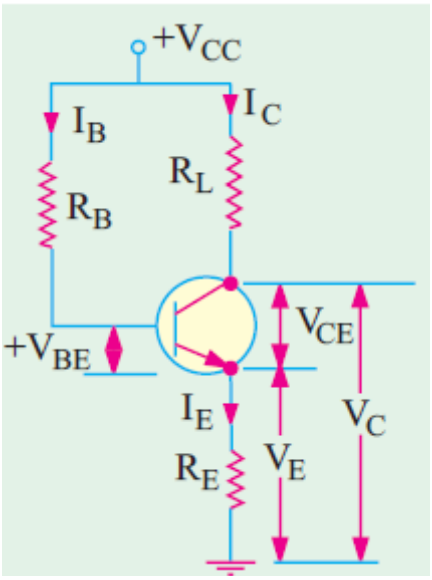
or $$V_{CC} = I_B R_B + V_{BE} + I_E R_E \qquad ...(i)$$

Now $I_B = I_C/\beta$ and $I_E \cong I_C$

Substituting these values in the above equation, we have

$$V_{CC} \cong \frac{I_C R_B}{\beta} + V_{BE} + I_C R_E$$

$$\therefore \qquad I_C \cong \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta} \cong \frac{V_{CC}}{R_E + R_B/\beta}$$ —neglecting VBE



3. collector-to-ground voltage $V_C = V_{CC} - I_C R_L$
4. emitter-to-ground voltage $V_E = I_E R_E \cong I_C R_E$
5. $$S = \frac{1 + R_B / R_E}{1 + R_B /(1+\beta) R_E} = \frac{1 + R_B / R_E}{1 + R_B / \beta R_E}$$
6. The β-sensitivity of this circuit is $K_\beta = \dfrac{1}{1 + \beta R_E / R_B}$

Base Bias with Collector Feedback

This circuit (Fig.) is like the base bias circuit except that base resistor is returned to collector rather than to the V_{CC} supply. It derives its name from the fact that since voltage for R_B is derived from collector, there exists a negative feedback effect which tends to stabilise I_C against changes in β . To understand this action, suppose that somehow β increases. It will increase I_C as well as $I_C R_L$ but decrease V_C which is applied across R_B. Consequently, I_B will be decreased which will partially compensate for the original increase in β .

(i) $I_{C(sat)} = V_{CC} / R_L$ —since $V_{CE} = 0$

(ii) $V_C = V_{CC} - (I_B + I_C) R_L \cong V_{CC} - I_C R_L$

Also, $V_C = I_B R_B + V_{BE}$

Equating the two expressions for V_C, we have

$I_B R_B + V_{BE} \cong V_{CC} \times I_C R_L$

Since $I_B = I_C / \beta$, we get

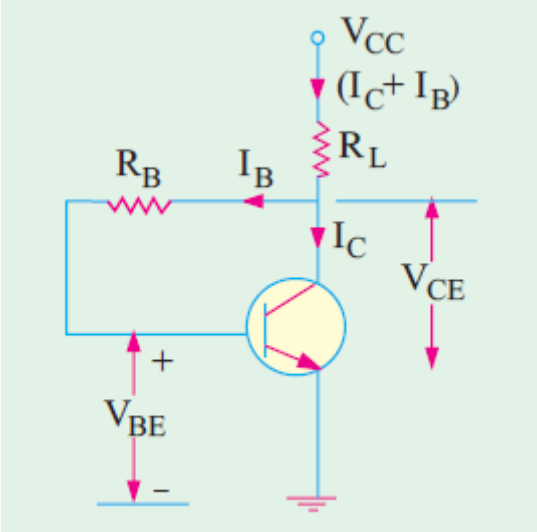
$$\frac{I_C}{\beta} . R_B + V_{BE} \cong V_{CC} - I_C R_L$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{BE}}{R_L + R_B / \beta} \cong \frac{V_{CC}}{R_L + R_B / \beta}$$

This is also the approximate value of I_E (again, we could take the help of β-rule). The β-sensitivity factor is given by

$$K_\beta = \frac{1}{\beta R_L / R_B} = 1 - \frac{I_C}{I_{C(sat)}}$$

$$S = \frac{1 + R_B / R_L}{1 + R_B /(1+\beta) R_L} \cong \frac{V_{CC}}{R_L + R_B / \beta}$$



Base Bias with Collector and Emitter Feedbacks

In the circuit of Fig., both collector and emitter feedbacks have been used in an attempt to reduce circuit sensitivity to changes in β. If β increases, emitter voltage increases but collector voltage decreases. It means that voltage across R_B is reduced causing I_B to decrease thereby partially off-setting the increase in β.

Under saturation conditions, V_{CC} is distributed over R_L and R_E.

Assuming I_B to be negligible as compared to I_C, we get, $I_{C(sat)} = V_{CC}/ (R_E + R_L)$.

$$\text{Actual value of } I_C \text{ is } = \frac{V_{CC} - V_{BE}}{R_E + R_L + R_B/\beta}$$

—going *via* R_B because V_{CE} is unknown.

$$V_C = V_{CC} - (I_C + I_B); \qquad R_L \cong V_{CC} - I_C R_L$$

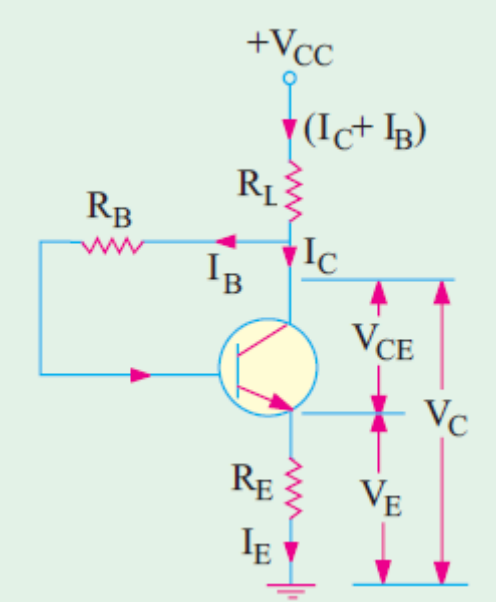
$$V_E = I_E R_E \cong I_C R_E; \quad \overline{V}_{CE} = V_C - V_E$$

$$V_{CE} \cong V_{CC} - I_C (R_L + R_E)$$

$$S = \frac{1 + R_B/(R_E + R_L)}{1 + R_B/\beta(R_E + R_L)}$$

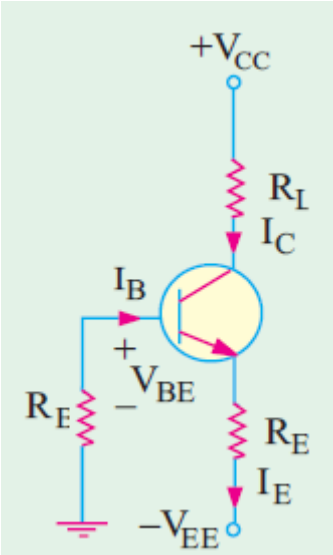
$$\text{It can be proved that } K_\beta = \frac{1}{1 + \beta(R_E + R_L)/R_B} = 1 - \frac{I_C}{I_{C(sat)}}$$

Obviously, K_β will be degraded with increase in R_B.



Emitter Bias with Two Supplies

This circuit gives a reasonably stable *Q*-point and is widely used whenever two supplies (positive and negative) are available. Its popularity is due to the fact that I_C is essentially independent of β.



It can be shown that $V_B \cong 0$ and $V_E = -V_{BE}$

Starting from ground and going clockwise round the base-emitter circuit, we get according to KVL.

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

or
$$I_B R_B + I_E R_E = V_{EE} - V_{BE} \qquad ...(i)$$

Now, $I_B = I_C/\beta \cong I_E/\beta$. Substituting this in (i) above we have

$$\frac{I_E R_B}{\beta} + I_E R_E = V_{EE} - V_{BE} \quad or \quad I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

If $V_{EE} \gg V_{BE}$ and $R_E \gg R_B/\beta$, $I_E = V_{EE}/R_B$.

If V_E is the emitter to ground voltage, then

$$-I_B R_B - V_{BE} - V_E = 0$$

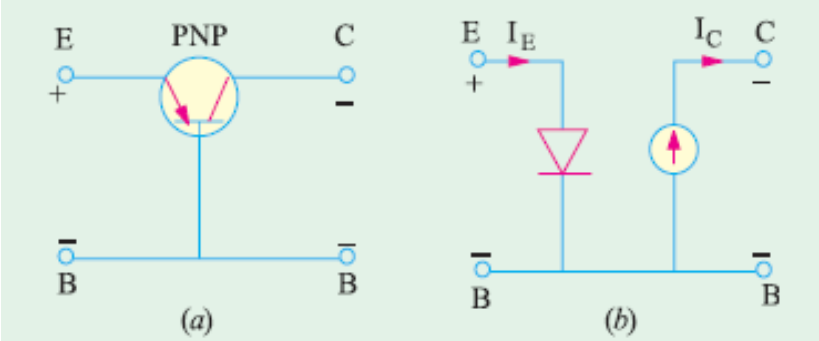
or
$$V_E = -(I_B R_B + V_{BE}) = -(V_{BE} + I_C R_B/\beta) \cong -V_{BE}$$

For this circuit, $S = \frac{1 + R_B/R_E}{1 + R_B/\beta R_E}$ and $K_B = \frac{1}{1 + \beta R_E/R_B}$

DC Equivalent Circuit

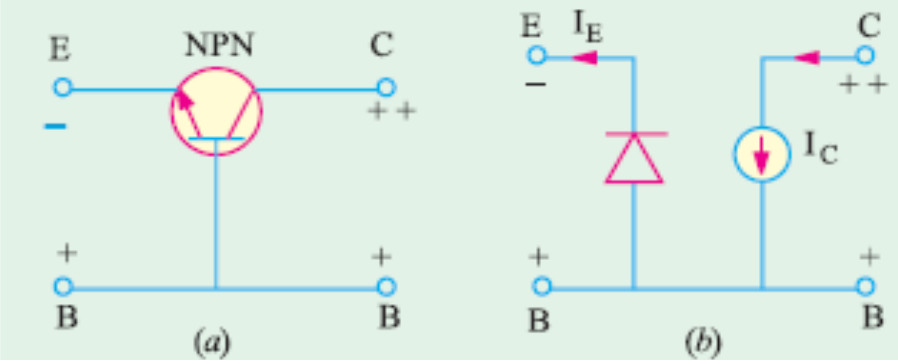
(a) CB Circuit

- In an ideal transistor, α = 1 which means that $I_C = I_E$.
- The emitter diode acts like any forward-biased ideal diode.
- However, due to transistor action, collector diode acts as a current source.
- The purpose of drawing dc equivalent circuit is to view an ideal transistor as nothing more than a rectifier diode in emitter and a current source in collector.
- In the dc equivalent circuit of Fig.(b), current arrow always points in the direction of conventional current.



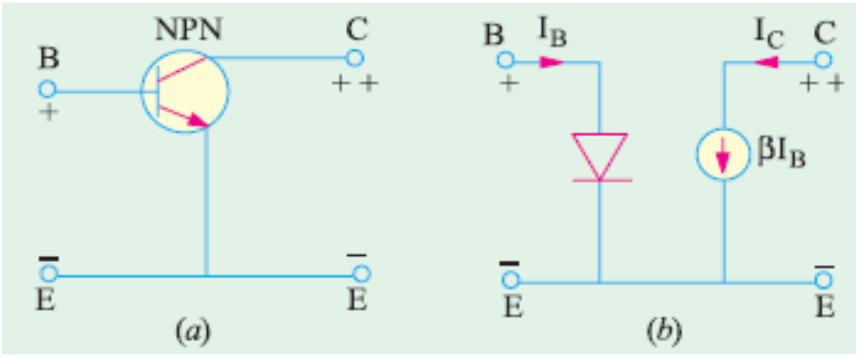
- As per the polarities of transistor terminals shown in Fig.(a), emitter current flow from E to B and collector current from B to C.

- The dc equivalent circuit shown in Fig. for an NPN transistor is exactly similar except that direction of current flow is opposite.



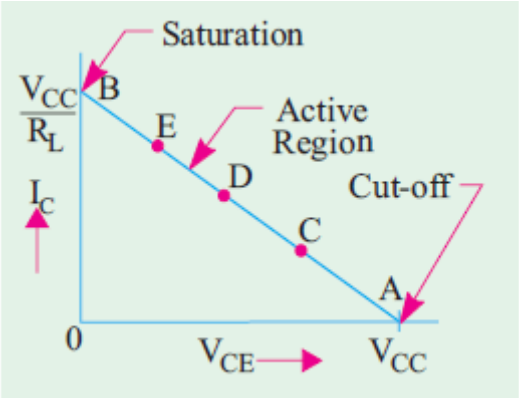
(b) CE Circuit

- Fig. shows the dc equivalent circuit of an NPN transistor when connectedin the CE configuration.
- As per the polarities of transistor terminals shown in Fig.(a), base current flow from B to E and collector current from C to E.
- In an ideal CE transistor, leakage current is ignored and a.c beta is considered as equal to dc beta.



DC Load Line

- DC load line of a transistor is a straight line jointing cut-off and saturation points.
- For the *CE* circuit, the load line is shown in figure and *A* is the cut-off point and *B* is the saturation point.



The voltage equation of the collector-emitter is

$$V_{CC} = I_C R_L + V_{CE} \quad \therefore \quad I_C = \frac{V_{CC}}{R_L} - \frac{V_{CE}}{R_L}$$

Consider the following two particular cases :

(*i*) when $I_C = 0$, $V_{CE} = V_{CC}$

— cut-off point A

(*ii*) when $V_{CE} = 0$, $I_C = V_{CC}/R_L$

— saturation point *B*

- The load line can be drawn if only V_{CC} and R_L are known
- Incidentally slope of the load line $AB = -1/R_L$
- The above given equation can be written as

$$I_C = \frac{V_{CE}}{R_L} + \frac{V_{CC}}{R_L}$$

- It is a linear equation similar to y = – mx + c
- The graph of this equation is a straight line whose slope is $m = -1/R_L$
- The cut-off point for this line is where $V_{CE} = V_{CC}$, also written as $V_{CE(cut\text{-}off)}$.
- Saturation point is given by $I_C = V_{CC}/R_L$, also written as $I_{C(sat)}$.

Active Region

- All operating points (like *C, D, E* etc. in Fig.) lying between cut-off and saturation points form the ***active region*** of the transistor
- In this region, *E*/*B* junction is forward-biased and *C*/*B* junction is reverse-biased (conditions necessary for the proper operation of a transistor)

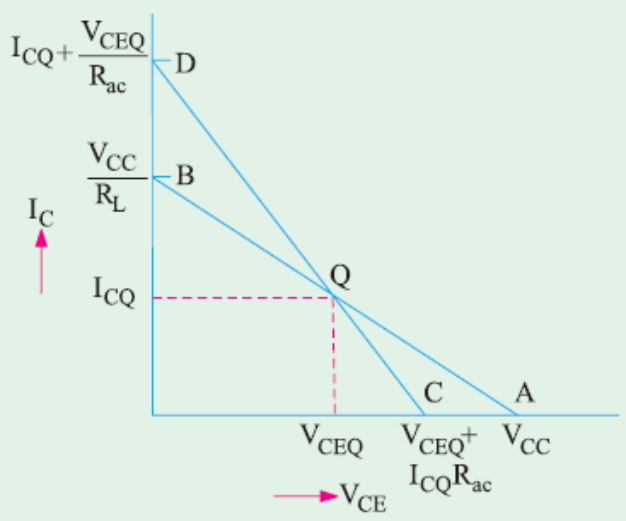
Quiescent Point

- It is a point on the dc load line, which represents the values of I_C and V_{CE} that exist in a transistor circuit when ***no input signal is applied***
- It is also known as the ***dc operating point or working point***
- The best position for this point is midway between cut-off and saturation points where $V_{CE} = \frac{1}{2}V_{CC}$ (like point D in Fig.)

AC Load Line

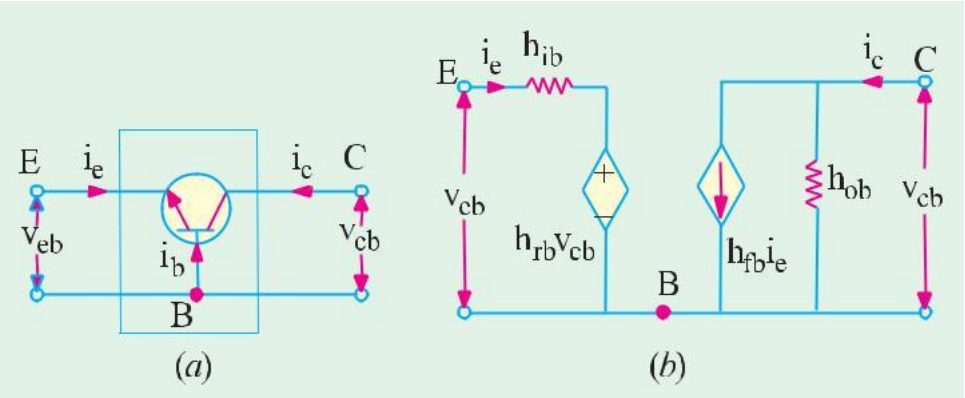
- It is the line along which Q-point shifts up and down when changes in output voltage and current of an amplifier

- This line is steeper than the dc line but the two intersect at the Q-point determined by biasing dc voltage and currents
- AC load line takes into account the ac load resistance whereas dc load line considers only the dc load resistance
- DC load line is represented by AQB
- The cut-off point is given by $V_{CE(cut\text{-}off)} = V_{CEQ} + I_{CQ}R_{ac}$ where R_{ac} is the ac load resistance*
- Saturation point is given by $I_{C(sat)} = I_{CQ} + V_{CEQ}/R_{ac}$.
- It is represented by straight line CQD in Fig.
- The slope of the ac load line is given by $y = \times 1/R_{ac}$
- It is seen from Fig. that maximum possible positive signal swing is = $I_{CQ}\,R_{ac}$
- Maximum possible negative signal swing is V_{CEQ}
- Peak-signal handling capacity is limited to $I_{CQ}\,R_{ac}$ or V_{CEQ} whichever is smaller



(a) Hybrid CB Circuit

In Fig.(a) an NPN transistor connected in CB configuration is shown.



Its ac equivalent circuit employing h-parameters is shown in Fig. (b).

The V/I relationships are given by the following two equations.

$$v_{eb} = h_{ib}\, i_e + h_{rb}\, v_{cb}$$

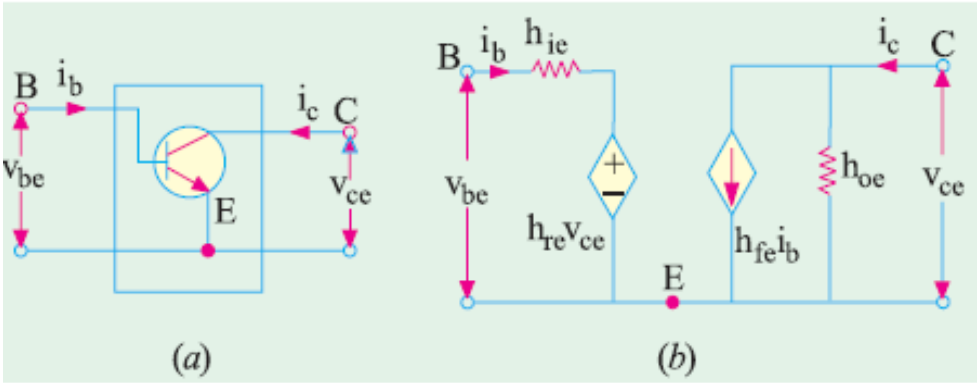
$$i_e = h_{fb}\, i_e + h_{ob}\, v_{eb}$$

- These equations are self-evident because applied voltage across input terminals must equal the drop over h_{ib} and the generator voltage
- Similarly, current i_c in the output terminals must equal the sum of two branch currents
- As per current convention, collector i_e is shown flowing inwards though actually this current flows outwards as shown by the arrow inside the ac current source
- Similarly, ac voltage polarities have been taken by considering upper terminal positive and lower one as negative
- It may be noted that no external dc biasing resistor or ac voltage sources have been connected to the equivalent circuit as yet.
- Incidentally, it may be noted that the ac equivalent circuit contains a Thevenin's circuit in the input and a Norton's circuit in the output.
- It is all the reason to call it a hybrid equivalent circuit

(b) Hybrid CE Circuit

- The hybrid equivalent of the transistor alone when connected in CE configuration is shown in Fig.
- Its V/I characteristics are described by the following equations

$$v_{be} = h_{ie}\, i_b + h_{re}\, v_{ec}$$
$$i_e = h_{fb}\, i_b + h_{oe}\, v_{ec}$$



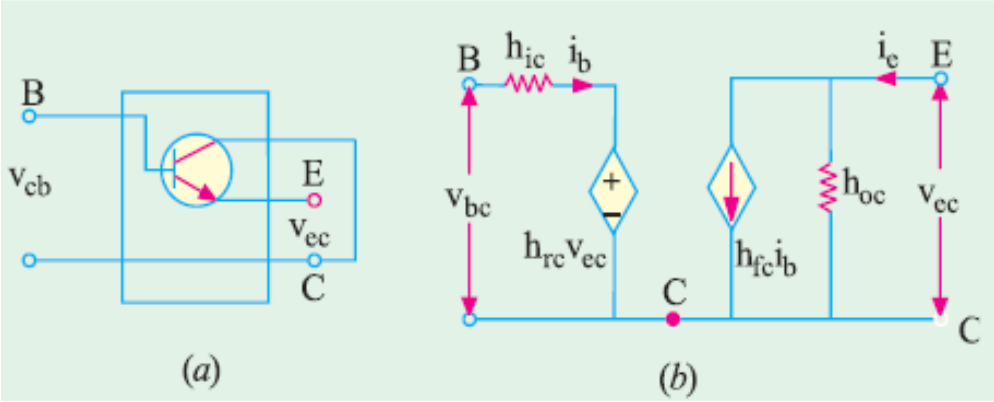
- Input signal source across its input terminals and load resistance across output terminals may be connected

(c) Hybrid CC Circuit

- The hybrid equivalent of a transis tor alone when connected in CC configuration is shown in Fig.

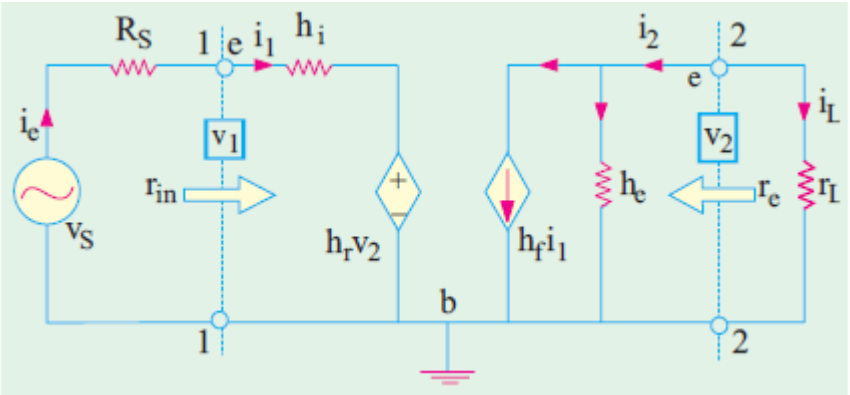
- Its V/I characteristics are described by the following equations

$$v_{be} = h_{ie} i_b + h_{re} v_{ec}$$
$$i_e = h_{fe} i_b + h_{oc} v_{ce}$$



- Input signal source across its input terminals BC and load resistance across output terminals EC may be connected in order to get a CC amplifier

Transistor Amplifier Formulae using *h*-parameters



- As shown in Fig., if we add a signal source across input terminals 1-1 of a transistor and a load resistor across its output terminals 2–2, we get a small-signal, low-frequency hybrid model of a transistor amplifier.
- It is valid for all the three configurations and holds good for all types of load whether a resistance of an impedance. We will now find expressions for its gains and impedances

  Before undertaking the above derivations, let us consider different components in the hybrid model of Fig.

- The input resistance looks like a resistance (h_i) in series with a voltage generator (h_r v_2)

- This generator represents the voltage feed-back from the output to the input circuit. It is known as voltage-controlled generator because its value is determined by v_2 (as h_r is a dimensionless constant)

- The output circuit also has two components:

  (i) h_0 component which represents the conductance as seen from output terminals and

  (ii) the current-controlled generator (h_f i_1) which simulates the transistor's ability to amplify. The parameter h_f is a dimensionless constant

The above model can be described mathematically by using the following two equations

Input Circuit

$$v_1 = \text{sum of voltage drops from } a \text{ to } b$$
$$= h_i i_1 + h_r v_2$$

Output Circuit

$$i_2 = \text{sum of currents leaving junction } c$$
$$= h_f i_1 + h_0 v_2$$

Now, $v_2 = -i_2 r_L$. Substituting this value in Eq. (*ii*) above, we have

$$i_2 = h_f i_1 - h_0 i_2 r_L$$

Eq. (*i*) and (*iii*) can now be used to find various gains of a transistor.

(*i*) Current Gain

It is given by $A_i = i_2/i_1$

Dividing both sides of Eq. (*iii*) by i_1, we get

$$\frac{i_2}{i_1} \quad h_f \quad h_0 \frac{i_2}{i_1} r_L \qquad \text{or} \qquad A_i = h_f - h_0 A_i r_L$$

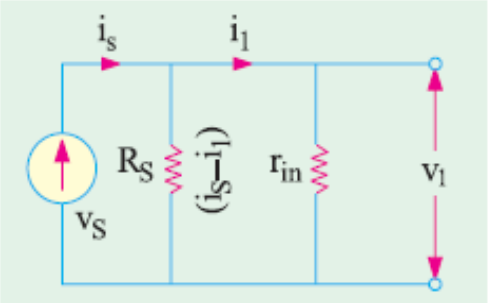
$$\therefore \qquad A_i \quad \frac{h_f}{1 \quad h_0 r_L}$$

If $r_L = 0$ or $h_0 r_L << 1$, then $A_i = h_f$

Current Gain Taking R_S into Account

- The source current is not the transistor input current because i_1 partly flows along R_S and partly along r_{in}.

- To illustrate this point, consider the Norton's equivalent of the source (Fig.).



- The overall current gain A_{is} is given by

$$A_{is} \quad \frac{i_2}{i_s} \quad \frac{i_2}{i_1} \quad \frac{i_1}{i_s} \qquad A_i \frac{i_1}{i_s}$$

$$i_1 \quad \frac{i_s R_s}{r_{in} \quad R_s} \qquad \text{or} \qquad \frac{i_1}{i_s} \quad \frac{R_s}{r_{in} \quad R_s}$$

$$\therefore \qquad A_{is} = \quad A_i . R_S / (r_{in} + R_S)$$

(ii) Input Impedance

- It is defined as the resistance when looking into the amplifier from its input terminals. Hence, $r_{in} = v_1/i_1$.

$$r_{in} \quad \frac{1}{i_1} \quad \frac{h_i i_1 \quad h_r \quad 2}{i_1} \qquad h_i \qquad h_r . \frac{2}{i_1}$$

Substituting the value of $v_2 = -i_2 r_L = -A_i \; i_1 r_L$, we get

$$r_{in} \quad h_i \quad h_i A_i r_L \quad h_i \quad \frac{h_f h_r r_L}{1 \quad h_0 r_L} \qquad h_i \quad \frac{h_f h_r}{h_0 \quad 1/r_L}$$

$$\frac{h_i \qquad h r_L}{1 \quad h_0 r_L} \qquad \text{where} \quad \Delta h = h_i h_0 - h_f h_r$$

$$\cong h_i \qquad - \text{if } h_r \text{ or } r_L \text{ is very small.}$$

It is seen that r_{in} depends on r_L *i.e.* ac resistance of the load across output terminals of the transistor.

(iii) Voltage Gain

- $A_v = v_2 / v_1$. It is also known as the internal voltage gain of the transistor.
- It is different from $A_{vs} = v_2 / v_s$ which is the gain from the source to the output terminals and is known as stage gain or overall gain.
- As seen from above, $v_2 = -A_i \, i_2 \, r_L$ and $v_1 = i_1 \, r_{in}$

$$\therefore \quad A_v \quad \frac{2}{1} \quad \frac{i_2 A_i r_L}{i_L r_{in}} \quad A_i \frac{r_L}{r_{in}}$$

$$\frac{h_f}{1 \quad h_0 r_L} \quad \frac{r_L (1 \quad h_0 . r_L)}{h_i \quad h . r_L} \quad \frac{h_f . r_L}{h_i \quad h . r_L}$$

$$\frac{h_f r_L}{h_i (1 \quad h_0 r_L) \quad h_f h_r r_L} \quad h_f \cdot \frac{r_L}{h_i}$$

Overall voltage gain is

$$A_{vs} \quad \frac{v_2}{s} \quad \frac{v_2}{v_1} \frac{v_i}{v_s} \quad A_v \frac{v_i}{v_s}$$

Now, v_s drops over series combination of R_S and r_{in}.

Drop across r_{in} constitutes v_1. Hence, $v_1 = v_s \times r_{in}/(R_S + R_{in})$

$$\therefore \quad \frac{v_1}{v_s} \quad \frac{r_{in}}{(R_S \quad r_{in})} \qquad \text{or} \qquad A_{vs} \quad A_v \frac{r_{in}}{(R_5 \quad r_{in})}$$

As seen, if $R_S = 0$, $A_{vs} = A_v$

Value of A_{vs} may also be obtained by adding R_S to h_i in the expression for A_v.

(iv) Output Impedance

It is defined as $r_0 \quad \frac{v_2}{i_2}\Big|_{v_s} \quad 0 \qquad \text{or} \qquad g_0 \quad \frac{i_2}{v_2}$

Dividing both sides of Eq. (*ii*) by v_2, we get

$$g_0 \quad h_f \cdot \frac{i_2}{v_2} \quad h_0$$

Taking V_s=0

$-i_1(h_i + R_S) - h_r v_2 = 0 \qquad \text{or} \qquad i_1/v_2 = -h_r/(h_i + R_S)$

Substituting this value in Eq. (*iv*) above, we have

$$g_0 \quad h_0 \cdot \frac{h_f h_r}{(h_i \quad R_S)} \quad \frac{h_o R_S \quad h}{(h_i \quad R_S)} \qquad \therefore \quad r_o \quad \frac{1}{g_o} \quad \frac{h_i \quad R_S}{h_o R_S \quad h}$$

It is seen that rin depends on r_L whereas ro depends on R_S.

If R_S is very large (*i.e.* circuit is driven by a current source) or h_r is negligible, then $r_o \cong 1/h_o$.

(v) Power Gain

$$A_p \quad \frac{P_2}{P_1} \quad \frac{v_2 i_2}{v_1 i_1} \quad A_v A_i \quad A_i^2 \frac{r_L}{r_{in}}$$

The above formulae are summarized as,

$$A_i \quad \frac{h_f}{1 \quad h_o r_L} \qquad h_f$$

$$A_i \quad \frac{h_f R_S}{(1 \quad h_o r_L)(r_{in} \quad R_S)} \qquad \frac{h_o R_S}{(r_{in} \quad R_S)}$$

$$r_{in} \quad h_i \quad \frac{h_f h_r r_L}{1 \quad h_o r_L} \qquad h_i$$

$$A_v \quad \frac{h_f h_r}{h_i \quad h.r_L} \qquad \frac{h_f r_L}{h_i} \; ; \; A_{vs} \quad \frac{h_f r_L}{(h_i \quad R_S)}$$

$$r_o \quad \frac{h_i \quad R_S}{h_o R_S \quad h} \qquad \frac{1 \quad h_i / R_S}{h_o \quad h / R_S} \qquad \frac{1}{h_o}$$

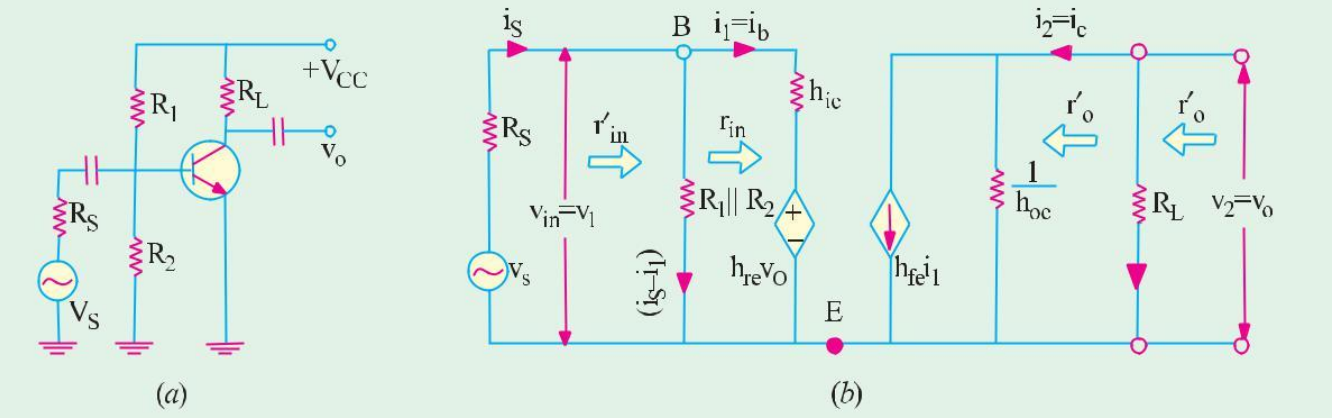
Typical Values of Transistor h-Parameters

Parameter	*CB*	*CE*	*CC*
h_i	25 Ω	1 K	1 K
h_r	3×10^{-4}	2.5×10^{-4}	≅ 1
h_f	–0.98	50	–50
h_o	0.5×10^{-6}S	25×10^{-6}S	25×10^{-6}S

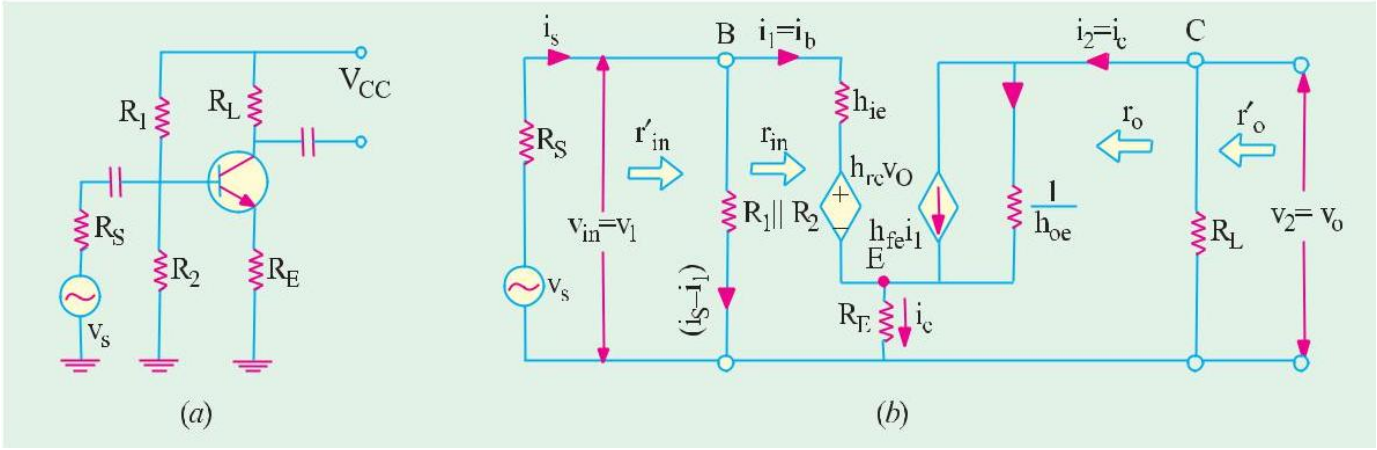
Common Emitter *h*-parameter Analysis

The h-parameter equivalent of the CE circuit of Fig.(a) is shown in Fig.(b).

In Fig.(a), no emitter resistor has been connected



However, Fig. below shows the CE circuit with an emitter resistor R_E.



1. Input Impedance

- When looking into the base-emitter terminals of the transistor, h_{ie} is in series with h_{re}
- For a CE circuit, h_{re} is very small so that h_{re} v_0 is negligible as compared to the drop over h_{ie}
- Hence, $r_{in}= h_{ie}$
- Ignoring $h_{re}v_o$,

$$v_1 = h_{ie}i_b + i_e R_E = h_{ie}\, i_b + (i_b + i)\, R_E$$
$$= h_{ie}i_b + i_b R_E + h_{fe}\, i_b R_E \qquad ((\quad i_c \quad h_{fe}i_b)$$
$$= i_b\,[h_{ie} + R_E(1 + h_{fe})]$$

$$\therefore \qquad r_{in} = r_{in(base)} = \frac{v_1}{i_1} \quad \frac{v_1}{i_b} \quad h_{ie} \quad (1 \quad h_{fe})R_E \ *$$

$$r_{in} \text{ or } r_{in(base)} = R_1 \| R_2 \| r_{in(base)}$$

2. Output Impedance

Looking back into the collector and emitter terminals of the transistor in Fig. (b),

$r_o \cong 1/h_{oe}$.

As seen, r_o' or $r_{o(stage)} = r_o \| R_L = (1/h_o) \| r_L \qquad (\quad r_L \quad R_L)$
Since $1/h_{oe}$ is typically 1 M or so and R_L is usually much smaller, $r_o' \cong R_L = r_L$

3. Voltage Gain

$$A_v \quad \frac{v_2}{v_1} \quad \frac{v_o}{v_{in}}$$

Now, $\quad v_o = - i_c R_L$ and $\qquad v_{in} \cong i_b h_{ie}$

$$\therefore \qquad A_v \quad \frac{i_s R_L}{i_b h_{ie}} \qquad \frac{i_c}{i_b} \cdot \frac{R_L}{h_{ie}} \qquad \frac{h_f R_L}{h_{ie}}$$

$$v_{in} = i_b[h_{ie} + R_E(1 + h_{fe})]$$

$$\therefore \quad A_v \quad \frac{v_o}{v_{in}} \quad \frac{i_c R_L}{i_b[h_{ie} \quad R_E(1 \quad h_{fe})]} \quad \frac{h_{fe} R_L}{h_{fe} \quad (1 \quad h_{fe}) R_E}$$

$$\frac{R_L}{R_E} \qquad \text{— if } (1 + h_{fe})\, R_E >> h_{ie}$$

4. Current Gain

$$A_i \quad \frac{i_2}{i_1} \quad \frac{h_{fe}}{1 \quad h_{oe} r_L} \quad h_{fe} \qquad \text{— if } h_{oe} r_L << 1$$

$$A_{is} \quad \frac{h_{fe} \,.\, R_1 \| R_2}{r_{in} \quad R_1 \| R_2}$$

5. Power Gain

$$A_p = A_v \times A_i$$

Common Collector *h*-parameter Analysis

The CC transistor circuit and its h-parameter equivalent are shown in Fig.

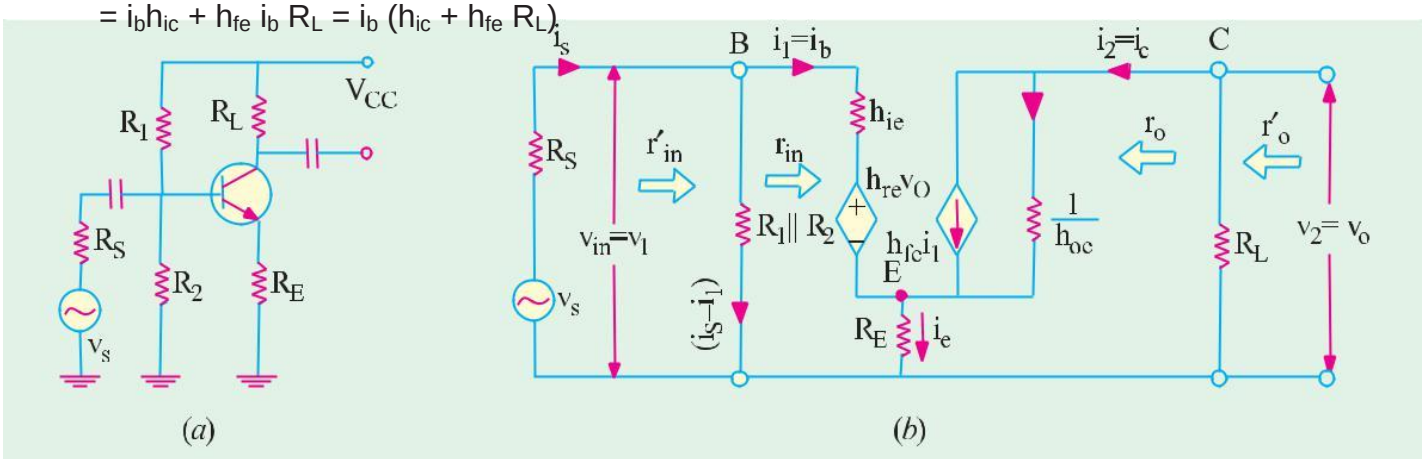
One can make quick approximations of CC gains and impedance if one remembers that

h_{re} = 1 i.e. all of v_o is fed back to the input (Art. 59.23).

1. Input Impedance

$v_{in} = i_b h_{ic} + h_{rc} v_o = i_b h_{ic} + v_o = i_b h_{ic} + i_e R_L$

$= i_b h_{ic} + h_{fe} i_b R_L = i_b (h_{ic} + h_{fe} R_L)$



$$\therefore \qquad r_{in} \quad \frac{v_{in}}{i_b} \quad h_{ic} \quad h_{fe} R_L$$

As seen, $r_{in(stage)} = r_{in(base)} \| R_1 \| R_2 = r_{in(base)} \| R_B$ where $R_B = R_1 \| R_2$

2. Output Impedance

$$r_o \quad \frac{v_2}{i_2}\Big|_{v_s\ 0} \qquad \frac{v_o}{i_c}\Big|_{v_s\ 0}$$

Now, $i_e \cong i_c = h_{fe} i_b = h_{fc} i_1$

Since $v_s = 0$, i_b is produced by $h_{rc} v_o = v_o$

Hence, considering the input circuit loop, we get

$$i_b \quad \frac{v_0}{h_{ic} \quad (R_S \parallel R_1 \parallel R_2)} \quad \frac{v_0}{h_{ic} \quad R_S \parallel R_B}$$

$$i_c \quad h_{fc} i_b \quad \frac{h_{fc} v_o}{h_{ic} \quad (R_S \parallel R_B)} \qquad \text{where } R_B = R_1 \parallel R_2$$

$$\therefore \qquad r_o \quad \frac{V_o}{i_e} \quad \frac{h_{ic} \quad (R_S \parallel R_1 \parallel R_2)}{h_{fe}}$$

Also, r_o' or $r_{o(stage)} = r_o \parallel R_L$

3. Voltage Gain

$$A_v \quad \frac{v_2}{v_1} \quad \frac{v_o}{v_{in}}$$

Now, $v_o = i_e R_L = h_{fe} i_b R_L$ and $i_b = (v_{in} - v_o) / h_{ic}$

$$v_o \quad \frac{h_{fe} R_L}{h_{ie}} (v_{in} \quad v_o) \quad \text{or} \quad v_o \quad 1 \quad \frac{h_{fe} R_L}{h_{ic}} \quad \frac{h_{fe} R_L v_{in}}{h_{ic}}$$

$$\therefore \qquad A_v \quad \frac{v_o}{v_{in}} \quad \frac{h_{fe} R_L / h_{ic}}{1 \quad h_{fe} R_L / h_{ic}} \quad 1$$

4. Current Gain

$$A_i \quad \frac{i_2}{i_1} \quad \frac{i_e}{i_b} \quad h_{fe}\ ; \ A_{is} \quad \frac{h_{fe} R_B}{r_{in} \quad R_B} \qquad \text{where } R_B = R_1 \parallel R_2$$

Approximate Hybrid Equivalent Circuits

- Low-frequency small-signal hybrid equivalent circuits after taking into account the 'feedback' voltage generator and output admittance
- In this, following two factors which exist in an actual transistor (as opposed to an ideal one) are taken into account

(i) There is a 'feedback' of the output voltage into the input voltage because of the transistor's non-unilateral behaviour,. This feedback is represented by a voltage-controlled generator $h_r v_2$ as shown in Fig.

By definition, an ideal amplifier is one which responds only to signals applied to its input terminals. It should not do the reverse i.e. reproduce at the input any portion of the ac signal applied at the output. Such an ideal one-way device is called a unilateral device. A real transistor cannot be unilateral because of unaviodable interaction between its input and output circuits. Therefore, not only its output responds to its input but, to a lesser degree, its input also responds to its output.

(ii) even when input circuit is open, there is some effective value of conductanece when looking into the transistor from its output terminals. It is represented by h_0.

Approximate hybrid formulae

The approximate hybrid formulas for the three connections are listed below. These are applicable when h_o and h_r are very small and R_S is very large. The given values refer to transistor terminals. The values of $r_{in(stage)}$ or r_{in}' and $r_{o(stage)}$ will depend on biasing resistors and load resistance respectively.

Item	*CE*	*CB*	*CC*
r_{in}	h_{ie}	h_{ib}	$h_{ic} + h_{fe}R_L$
ro	$\frac{1}{h_{oc}}$	$\frac{1}{h_{oB}}$	$\frac{h_{ie}}{h_{fc}}$
A_i	$h_{fe} = \beta$	$-h_{fb} \cong 1$	$-h_{fe} \cong \beta$
A_v	$\frac{h_{ie}R_C}{h_{is}}$	$\frac{f_{fb}}{h_{ib}}R_C$	1