SATHYABAMA INSTITUTE OF SCIENCE AND TECHNOLOGY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

COURSE MATERIAL

Subject Name : Digital Communications Subject Code : SEC1313

UNIT IV - SYNCHRONAIZATION

1.INTRODUCTION

1.1 Synchronization costs and benefits

2. Frequency and phase synchronization (Carrier Synchronization)

2.1Steady state tracking characteristics.

2.2 Carrier synchronization using Mth power loop

2.3 Suppressed of carrier loops

2.4 Costas loop

2.5 Higher order suppressed carrier loops

3. Symbol synchronization (clock recovery)

3.1 Open loop symbol synchronizers

3.2 Closed loop symbols synchronizers

4. Frame synchronization

5. Network synchronization

5.1 Open loop network synchronization techniques

5.2 Closed loop network synchronization techniques

6. Tracking and Acquisition in spread spectrum system

6.1 Acquisition in spread spectrum system

6.2 Serial search

6.3 Parallel search

7. Tracking Techniques

7.1 Matched filter energy detector

7.2 Radiometer

1. INTRODUCTION

The signals from various sources are transmitted on the single channel by multiplexing. This requires synchronization between transmitter and receiver. So the transmitter and Receiver is said to be synchronous when an event occur simultaneously in both transmitter and receiver at a particular instant of time. The process of making a situation synchronous and maintaining it in this condition is called synchronization.

If special synchronization bits are added in the transmitted signal for this purpose means it is known as transmitter synchronization.

Synchronization is also required for detectors to recover the digital data properly from the modulated signal. In almost every receiver or demodulator performance, some level of signal synchronization is used. If the parameters are adjusted at the receiver environment for synchronous then it is called receiver synchronization. For example in the case of coherent phase demodulation (PSK), the receiver is assumed to be able to generate reference signals whose phases are identical (except perhaps for a constant offset) to those of the signaling alphabet at the transmitter.

Digital communication systems using coherent modulation require three levels of synchronization 1-Phase, 2-Symbol, 3-Frame synchronization. (2&3 combinely known as Time synchronization)

Digital communication systems using noncoherent modulation require two levels of synchronization 1-Frequency, 2-Symbol, 3-Frame synchronization.

Since the modulation is not coherent, accurate phase lock is not required. Instead, noncoherent require frequency synchronization. Frequency synchronization differs from phase synchronization in that the replica of the carrier that is generated by the receiver is allowed to have arbitrary constant phase offset from the received carrier. Receiver designs can be simplified by removing the requirement to determine the exact value of the incoming carrier phase.

In digital communication systems, the receiver, has accurate knowledge about incoming symbol Time period. This knowledge is required in order to know the proper symbol integration interval (the interval over which energy is integrated prior to making symbol decision).

It can be seen that symbol synchronization and phase synchronization are similar in that both involve producing in the receiver a replica of a portion of the transmitted signal.

For phase synchronization, it is an accurate replica of the carrier.

For symbol synchronization, it is a square wave at the symbol transition rate (the receiver

must be able to produce a square wave for each incoming signals transitions between symbols). A receiver that is able to do this can be said to have symbol synchronization, or to be in symbol lock.

In many communication systems an even higher level of synchronization is required. This is usually called frame synchronization. Frame synchronization is required when the information is organized in blocks, or messages of some uniform number of symbols (this occur, for example, if a block code is used for forward error control, or if the communication channel is used for several user as in TDMA). In the case of block coding, the decoder needs to know the boundaries between code words in order to decode the message correctly. In the case TDMA, it is necessary to know where the location of boundaries between channel users are, in order to route the information correctly.

Similar to symbol synchronization, frame synchronization is equivalent to being able to generate a square wave at the frame rate, with the zero crossing coincident with the transitions from one frame to the next.

All of the discussion thus far had been oriented toward the receiving end of a communication link. There are many cases, when the transmitter assumes the more active role in synchronization by varying the time and frequency of its transmissions to receiver, as in the case of satellite communication network. In most of these cases, the transmitter knows on a return path from the receiver to determine the accuracy of its synchronization (two way communications are used in the transmitter synchronization). The transmitter synchronization is often called network synchronization.

1.1 Synchronization costs and benefits

- The most obvious costs is in the need for additional hardware or software in the receiver for acquisition and tracking.
- Extra time is required to achieve synchronization before commencing communications.
- Error control coding is used.

2. Frequency and phase synchronization (Carrier Synchronization)

The carrier synchronization is required in coherent detection methods to generate a coherent reference at the receiver. In this method the data bearing signal is modulated on the carrier in such a way that the power spectrum of the modulated carrier signal contains a discrete component at the carrier frequency. That is the Fourier transform of the modulated signal contains one component at fc also. Then the phase lock loop can be used to track this component fc. the output frequency of

phase locked loop is thus locked to the carrier frequency fc in the transmitted signal. This output frequency of phase locked loop is used as a coherent reference signal for detection in the receiver.

The heart of all synchronization circuits is the phase locked loop (PLL). A schematic diagram of the basic PLL is shown in fig. PLL is a servo control loop, whose controlled parameter is the phase of a locally generated replica of the incoming carrier signal. PLL has three basic components:-

Phase detector: is a device that produce a measure of the difference in phase between an incoming signal and the local replica. As the incoming signal and the local replica change with respect to each other, the phase difference (or phase error) becomes a time varying signal into the loop filter.

Loop filter: is the device governs the PLL response to these variations in the error signal.

VCO: is the device that produces the carrier replica. The VCO is a sinusoidal oscillator whose frequency is controlled by a voltage level at the device input. In figure the phase detector is shown as a multiplier, the loop filter is described by its impulse response function f(t), with Fourier transform F(w), and the voltage controlled oscillator (VCO) is also indicated. A VCO is an oscillator whose output frequency is a linear function of its input voltage over a certain range. The output of VCO may be a digital signal (i.e not a sinusoidal), but it may be implemented as a read only memory whose output frequency controlled by a combination of a clock and the error signal (as a variable address).

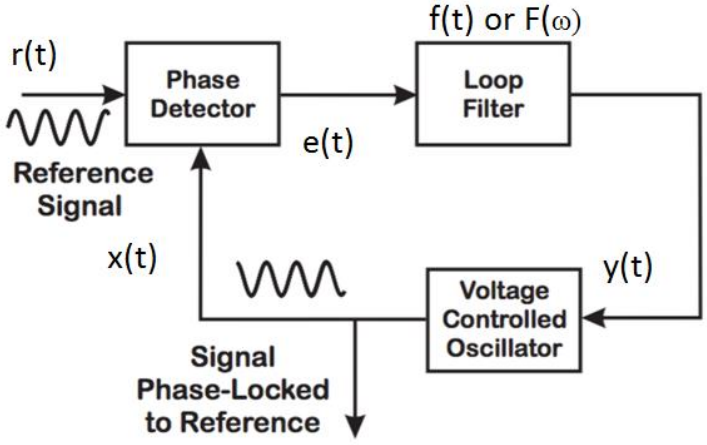


Figure 1. Basic PLL

Let us consider the input signal to the PLL is given by

$$r(t) = 2\,cos[\,\omega_0 t + \theta(t)]$$

Where $\omega_0 t$ is the nominal carrier frequency and θ(t) is a slowly varying phase. Similarly, consider a normalized VCO output of the form .

$$x(t) = 2\,sin[\,\omega_0 t + \hat{\theta}(t)]$$

Where $\hat{\theta}(t)$ is the estimated phase.

These signals will produce an output error signal at the phase detector output of the form

$$e(t) = x(t)r(t) = 2\,sin[\,\omega_0 t + \hat{\theta}(t)]\,] * 2\,cos[\,\omega_0 t + \theta(t)]$$

$$e(t) = x(t)r(t) = sin[\,\theta(t) - \hat{\theta}(t)] + sin[\,2\omega_0 t + \theta(t) + \hat{\theta}(t)]$$

Assuming that the loop filter is low pass filter, the second term will be filtered out. Thus the low pass filter provides error signal that is a function of the difference phases between input and the output, only. This error signal is applied to the input VCO. The VCO output frequency is the time derivative of the argument (angle) of the sine function. If we assume that ω_0 is the output frequency of the VCO when the voltage is zero, we can express the difference in the VCO output frequency from ω_0 as the differential of the phase term $\hat{\theta}(t)$.

Therefore, since an input voltage of zero produces an output frequency of ω_0, the difference in the output frequency ω_0 form will be proportional to the value of the input voltage y(t).

$$\Delta\omega(t) = \frac{d}{dt}\left[\hat{\theta}(t)\right] = K_0 y(t) = K_0 e(t) * f(t)$$

$$\approx K_0[\,\theta(t) - \hat{\theta}(t)] * f(t)$$

Where Δω(t)=the frequency difference, *= convolution, K_o= the gain the VCO

f(t)=the loop filter impulse response

This linear differential equation in $\hat{\theta}(t)$ (if small angle approximation) is known as the linearized loop equation. It is used to determine the loop behaviour during normal operation (where the phase error is small). Consider the Fourier transform of above equations

$$F\frac{d[\hat{\theta}(t)]}{dt} = F\{K_0[\theta(t) - \hat{\theta}(t)] * f(t)\}$$

$$jW\hat{\theta}(\omega) = K_0[\theta(\omega) - \hat{\theta}(\omega)]F(\omega)$$

$$\hat{\theta}(\omega)\,[j\omega + K_0 F(\omega)] = K_0\,\theta(\omega)F(\omega)$$

$$\frac{\hat{\theta}(t)}{\theta(t)} = \frac{K_0\, F(\omega)}{j\omega + K_0\, F(\omega)} = H(j\omega)$$

Where H(jω)is the closed loop transfer function of the PLL

Example :

Show that for appropriately chosen K_0 , and f(t) the linearized loop equation (for PLL) demonstrates a tendency toward phase lock-that is, the phase difference between the incoming signal and the VCO output tends to decrease.

Solution

$$\Delta\omega(t) \approx K_0[\,\theta(t) - \hat{\theta}(t)] * f(t)$$

1. Consider the case where the phase of the input signal is θ(t) slowly varying with time.
2. If the phase difference on the right hand side of above equation is positive [i.e θ(t) > $\hat{\theta}(t)$], so that (t) will increase with time, which will tend to reduce the magnitude of the difference θ(t) - $\hat{\theta}(t)$
3. If θ(t) = $\hat{\theta}(t)$ then the equation indicates that $\hat{\theta}(t)$ will not change with time ,and the equality will be maintained.

2.1 Steady state tracking characteristics.

By using above equation we can obtain an expression for the Fourier transform of the phase error E(w)

$$\frac{\hat{\theta}(\omega)}{\theta(\omega)} = \frac{K_0\, F(\omega)}{j\omega + K_0\, F(\omega)} = H(j\omega)$$

$$E(w) = Fe(t) = \left[\theta(\omega) - \hat{\theta}(\omega)\right]$$

$$= [1 - H(\omega)\theta(\omega)]$$

$$= \frac{j\omega\theta(\omega)}{j\omega + K_0\, F(\omega)}$$

The above equation can be used to determine the steady state error response of a loop to a variety of possible input characteristics. The steady state error is the residual error after all transients have died away.

$$log_{t\to\propto}\, e(t) = log_{j\omega\to}\, j\omega E(\omega)$$

2.2 Carrier synchronization using Mth power loop

Fig 2 shows the block diagram of carrier recovery or carrier synchronization circuit.

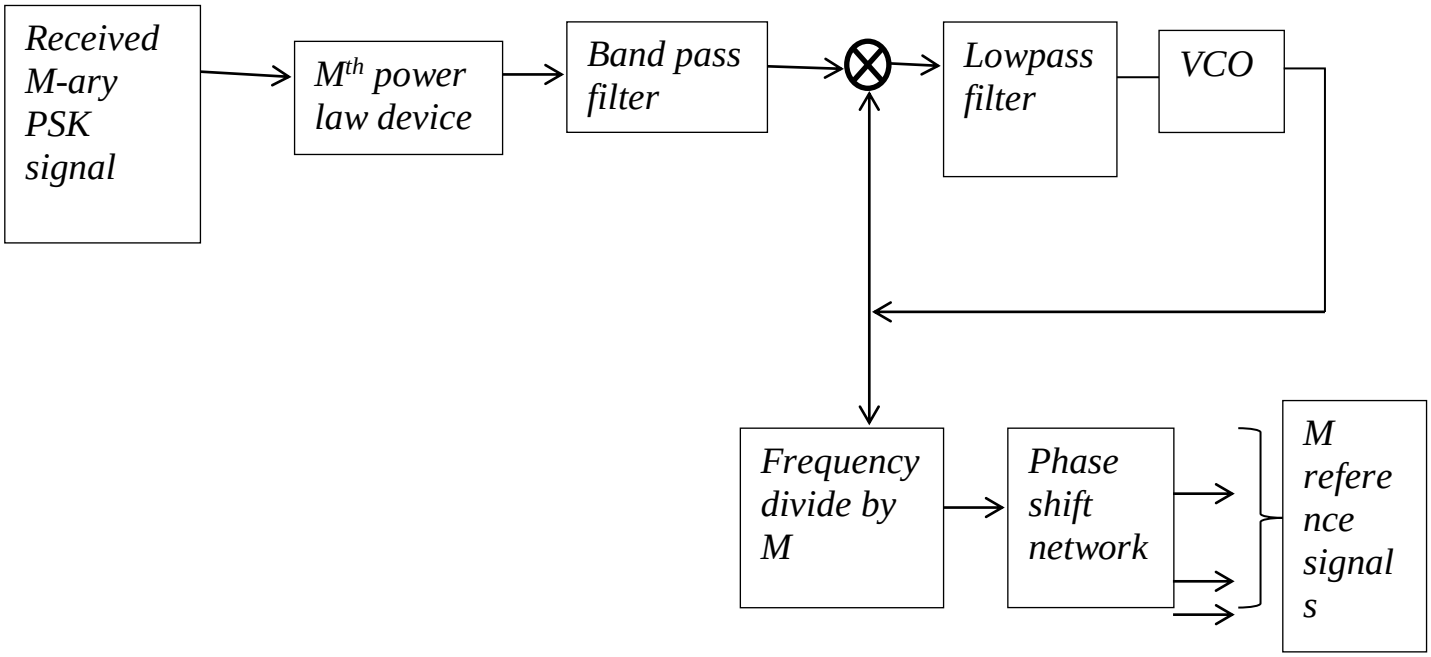


Fig 2: Block diagram of Mth power loop

Fig 2 shows the block diagram of carrier recovery circuit for M-ary PSK*. This circuit is called the Mth power loop. When M = 2, then it is called squaring loop. When M = 2, the M-ary PSK is then called as binary PSK. As shown in diagram, the input signal is first raised to the Mth power by the mth power law device with the frequency fc. The phase locked loop consists of a phase detector, low-pass filter and VCO. The phase locked loop tracks the carrier frequency. Then the output of a voltage controlled oscillator (VCO) is the carrier frequency. The output frequency of VCO is divided by M. this is done because the Mth power of the input signal multiplies carrier frequency by M. the phase shift network then separates 'M' reference signals for the 'M' correlation receivers. In this technique the power of the input signal is raised to some power say 'M'. Let us say M = 2, then the input signal is squared. Because of this, the sign of the recovered carrier is always independent of sign of the input signal carrier since it is squared. Therefore there can be 180 degree error in the output.

2.3 Suppressed of carrier loops

In the case of a phase modulation, if the carrier phase variation due to the modulation less than $\pi/2$ radians, there will be positive energy at the carrier frequency. This is called a system design that has a residual carrier component. A diagram of the signal space for a binary phase modulated with a residual carrier components is shown in figure, for modulating angle of $\gamma \leq \pi/2$. However, the residual component is wasted energy, it is not to transmit the information, only to transmit the carrier. Thus most modern phase modulated systems are suppressed carrier systems. This means that there is no average energy transmitted at the carrier frequency also there is no longer any signal for the basic PLL of figure to track.

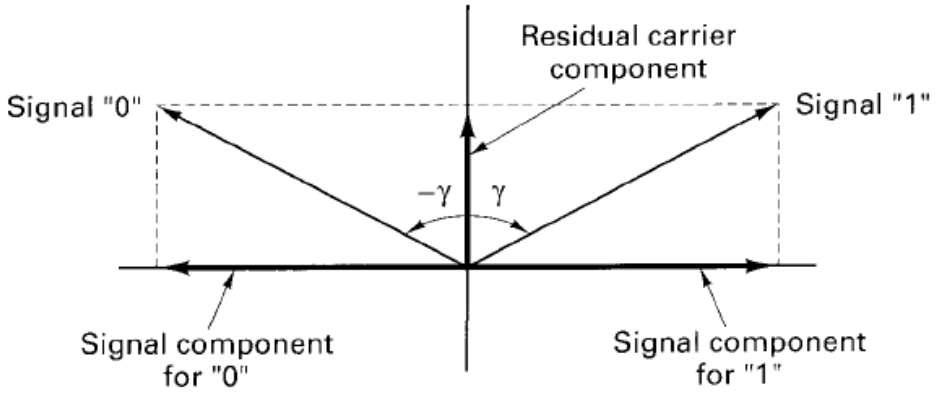


Figure 3 Residual Carrier

Consider, as an example, a BPSK

$$r(t) = m(t)\,sin(\omega_0 t + \theta) + n(t)$$

Where m(t)= 1 with equal probability. This is suppressed carrier with the average energy at radian frequency ω_0 is zero. This represented graphically in above figure when $\gamma \leq \pi/2$, and in this case the residual carrier will vanish.

To acquire and track the phase of the carrier, the effects of the modulation must be eliminated. One way to eliminate the modulation is to square the signal.

$$r^2(t) = m^2(t)sin^2(\omega_0 t + \theta) + n^2(t) + 2n(t)m(t)sin(\omega_0 t + \theta)$$

$$r^2(t) = \frac{1}{2} - \frac{1}{2}cos(2\omega_0 t + 2\theta) + n^2(t) + 2n(t)m(t)sin(\omega_0 t + \theta)$$

If $m^2(t) = 1$, the second term on the right hand side of above equation is a carrier related term(at twice the original carrier frequency) that can be acquired and tracked with a basic PLL of the type illustrated in figure 1 Such an arrangement is illustrated in figure 4.

The problems with this schematic are:-

- All phase angles have been doubled. Thus, the phase noise and phase jitter have been doubled.
- Larger S/N is required for this PLL to overcome this larger internal variation of the noise.
- False lock. This additional loss due to the terms in above equation $n^2(t)2n(t)m(t)sin(\omega_0 t + \theta)$ which is called the loop squaring loss (SL)

is given by

$$\frac{S_L}{S} \leq 1 + \frac{N_o B_i}{S}$$

Where S is the signal power, B_i is the filter bandwidth and N_o is the single sided power spectral density of the prefiltered, white Gaussian noise process.

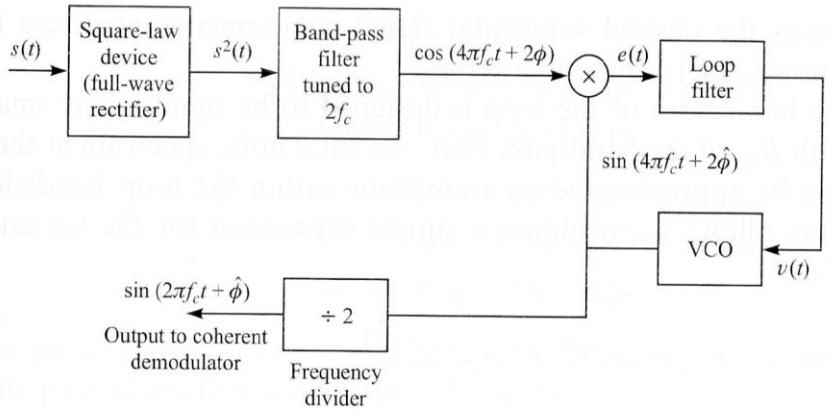


Figure 4 Suppressed of carrier loops

$\frac{S_L}{S} \leq 1 + \frac{1}{2P_i}$ Where Pi is the signal to noise ratio

2.4 Costas loop

This loop design is important because it eliminates the square law device, which can be difficult to implement at carrier frequencies, and replaces it with a multiplier and relatively simple low pass filters. The problem in this loop is to implement the two LPF identical. This problem can be solved by using the digital filter.

The decision as to whether to implement a Costas loop or the classical design of figure 5 amount to a design decision between the difficulty of implementing the squaring device and the difficulty of implementing closely matched arm filters.

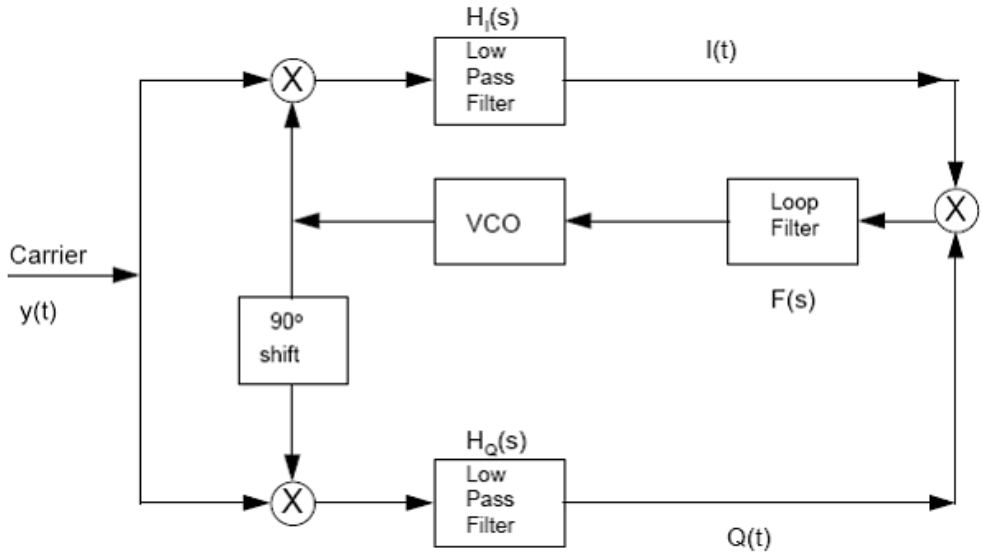


Figure 5 Costas loop

½ $\frac{\sqrt{2E}}{T}$cos $(\varphi - \theta)$ and ½ $\frac{\sqrt{2E}}{T}$sin $(\varphi - \theta)$.The multiplier output is given as,

Vm= ¼ x 2E/T sin $(\varphi - \theta)$cos $(\varphi - \theta)$

= E/ 2T. ½ sin2 $(\varphi - \theta)$

= E/4Tsin2 $(\varphi - \theta)$

The power 'P' of the signal over the period T is given by,

P = E/T

Therefore equation Vm can be written as,

Vm = P/4 sin2 $(\varphi - \theta)$

If there is some difference between the VCO frequency and the input carrier frequency then the phase difference $(\varphi - \theta)$ is changed proportionally. The change in $(\varphi - \theta)$ causes Vm to increase or decrease VCO frequency such that synchronization is maintained.

2.5 Higher order suppressed carrier loops

Squaring the signal a second time (equivalent to taking the original signal to the fourth power) can be seen to produce a term with a carrier component at four times the transmitted carrier's frequency. The loss for fourth power loop is

$$S_L \leq 1 + \frac{9}{\rho_i} + \frac{6}{{\rho_i}^2} + \frac{3}{2{\rho_i}^3}$$

Example

Compare and discuss the results of the upper bounds on squaring loss (S_L) for second and forth loops (used for receiver synchronization) if the input loop signal to noise ratio Pi is 10 dB.

Solution :

$$10\ dB = 10\ log \frac{S}{N}$$

$$\frac{S}{N} = 10 = P_i$$

For the squaring loop :

$$S_L = 1 + \frac{1}{2P_i} = 1 + \frac{1}{2 * 10} = 1.05$$

$$= 10\ log\ 1.05 = 0.2dB$$

For the fourth loop :

$$S_L \leq 1 + \frac{9}{\rho_i} + \frac{6}{{\rho_i}^2} + \frac{3}{2{\rho_i}^3}$$

$$S_L \leq 1 + \frac{9}{10} + \frac{6}{10^2} + \frac{3}{2 * 10^3} = 10 + 0.06 + 0.0015 = 1.9165$$

$$10\ log\ 1.9165 = 2.9dB$$

Thus, an input signal to noise ratio of 10dB is suitable to keep losses small for the squaring loop, the same signal to noise ratio may allow significant losses for the fourth power loop.

3. Symbol synchronization (clock recovery)

In the last section we have seen how to recover the carrier for coherent detection. In a matched filter or correlation receiver, the incoming signal is sampled at the end of one bit or symbol duration. This is because the output of matched filter is maximum at tm = T. here T is the symbol or bit duration. Therefore the receiver has to know the instants fo time at which a symbol or bit is transmitted. That is the instants at which a particular bit or symbol starts and when it is ended. The estimation of these times of bit or symbol is called symbol or bit synchronization. The symbol or bit

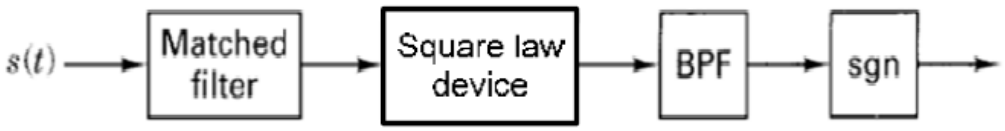
timing is controlled by a clock at the transmitter. The receiver has to know the phase of this clock. Therefore symbol or bit synchronization is also called clock recovery.

The symbol synchronizers can be classified into two basic groups according to the type of the loop:-

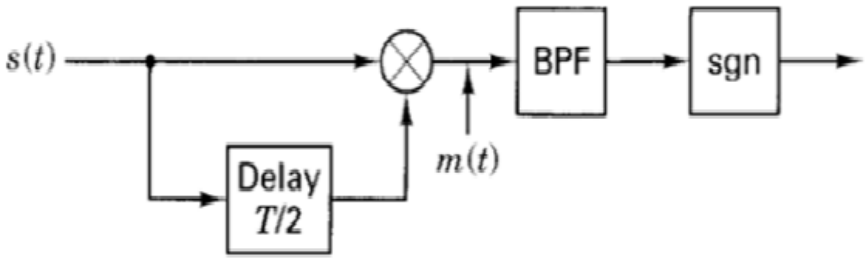
1. Open loop synchronizers: These circuits recover a replica of the transmitter data clock output directly from operation on the incoming data stream.
2. Closed loop synchronizers: These synchronizers attempt to lock a local data clock to the incoming signal by use of comparative measurements on the local and incoming signals.

3.1 Open loop symbol synchronizers -Open loop symbol synchronizers are also called filter synchronizers.

This class of synchronizers generates a frequency component at the symbol rate by operating on the incoming baseband sequence with a combination of filtering and a nonlinear device. In this synchronizer, the desired frequency component, at the data symbol rate, is filtered by the bandpass filter, and shaped with a high gain saturating amplifier. The shaping recovers the square wave appearance of the data clock signal. Three examples of open loop bit synchronizers are shown in Following figures



(a)



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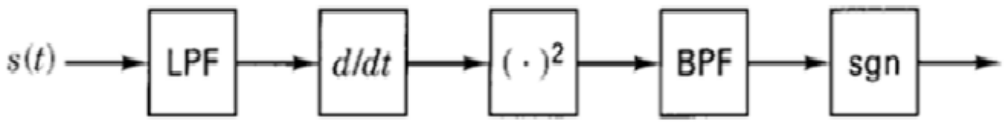


(c)

In the first example the incoming signal is filtered with matched filter and rectified by the square device. The output waveform from square law device will contain a Fourier component at the fundamental frequency of the data clock. This frequency is filtered by BPF and shaped with an ideal saturating amplifier, with transfer function (signum function)

$$Sgn(t) = \begin{cases} 1 & for \quad t \rangle 0 \\ 0 & \quad\quad t = 0 \\ -1 & \quad\quad t \langle 0 \end{cases}$$

The second example shown in figure produces a Fourier component at the data clock frequency by means of a delay and multiply. The delay show in figure is half a bit period, which is the best value because it provides the strongest Fourier component.

The third example with the main operations are those differentiation and rectification by using a square law device. For a square wave input, the differentiator will produce positive or negative spikes at all symbol (bit) transitions. when rectified, the resulting sequence of positive spikes will have a Fourier component at the data symbol (bit) rate.

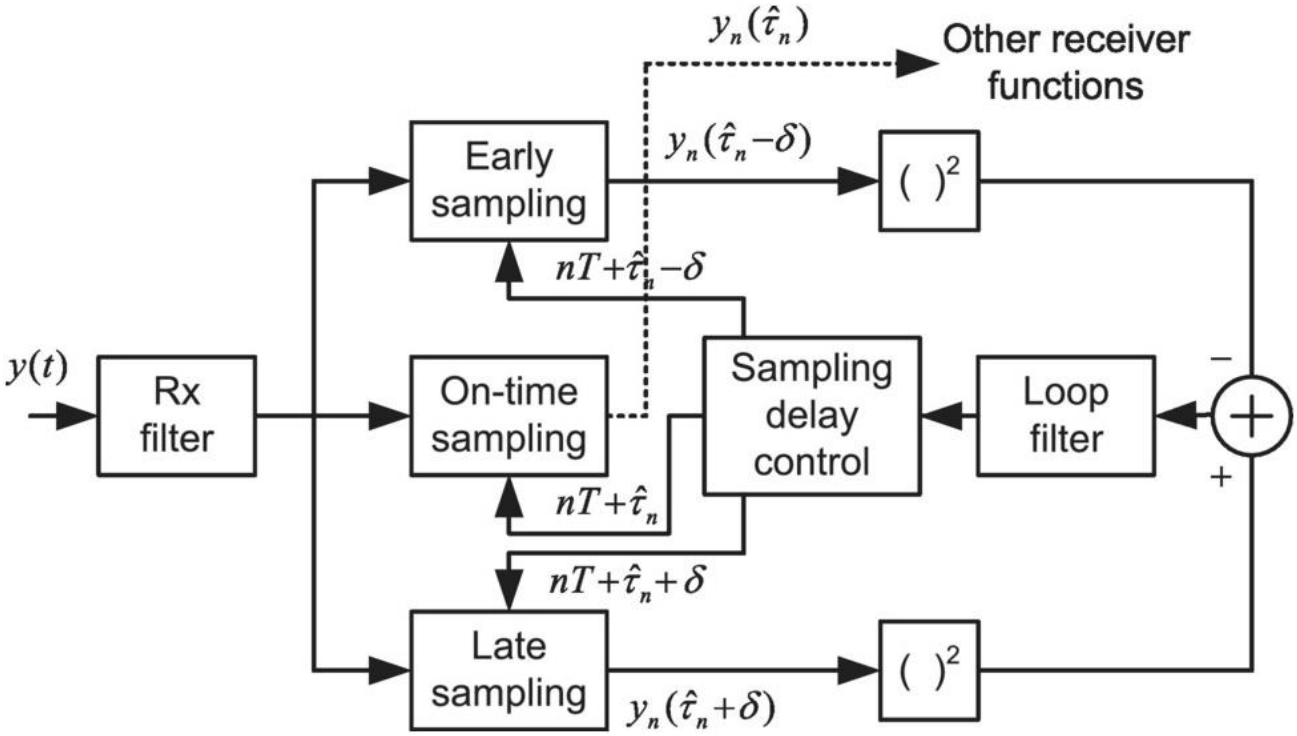
3.2 Closed loop symbols synchronizers

The primary disadvantage of open loop symbol synchronization methods is that there is an unavoidable non-zero mean tracking. Closed loop, symbol data synchronizers use comparative measurements on the incoming signal and a locally generated data lock signal to bring the locally generated signal into synchronism with incoming data transitions.

Early Late Synchronizer

The most popular of the closed loop symbol synchronizers is the early/late gate synchronizer as shown in following figure. The synchronizer operates by performing two separate integrations of the incoming signal energy over two different(T-d) second portions of a symbol interval. The first integration (the early gate) begins from zero to T-d. The second integration (the

late gate) begins from d to T. The difference in the absolute values of the outputs of these two integrations Yx and Yz is a measure of the receiver's symbol timing error, and it can be fed back to the loop's timing reference to correct loop timing.



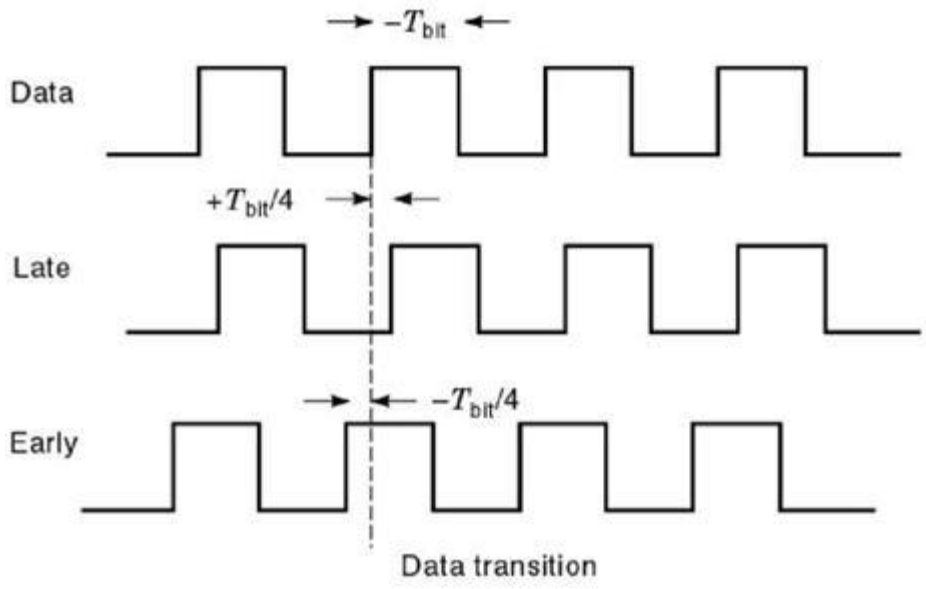


Fig shows the block diagram of early late synchronizer. This type of synchronizer does not need any zero crossings. We know that in the matched filter the output is maximum at the sampling time. Actually the sampling time is obtained by bit synchronization. The prefix allows the time for bit sync acquisition and indicates the beginning of a frame. After the prefix, there is one more codeword. It indicates the start of message. The message bits follow the special codeword. To maintain the synchronization of message bits, the sync words are inserted periodically in the bit stream.

Disadvantages:

If there is a long string of 1's or 0's, then y(t) has no zero crossings and synchronization may be lost.

If zero crossing of y(t) are not placed at integer multiples of Tb, the synchronization suffers from timing jitter.

4. Frame synchronization

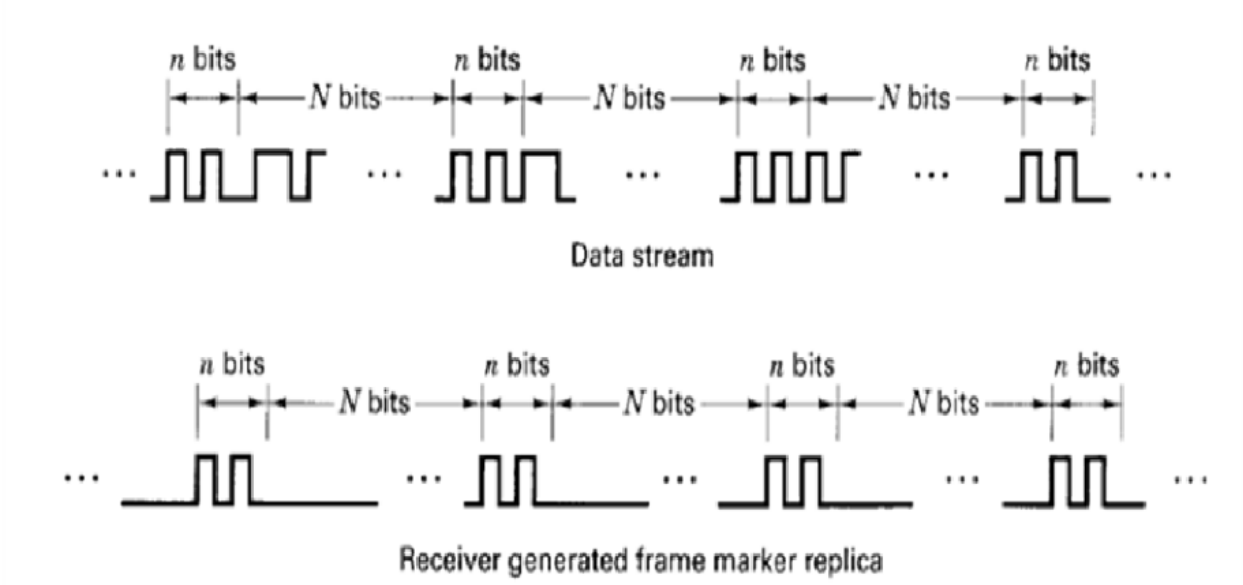
All digital data streams have some sort of frame structure. The data streams is organized into uniformly sized groups of bit as shown previously. Computer data are typically organized into words of some number of 8 bit bytes. To receive the incoming data stream, the receiver needs to be synchronized with the data stream's frame structure.

Frame synchronization is usually accomplished with the aid of some special signaling procedure from the transmitter.

The simplest frame synchronization aid is the frame marker shown in following figure. The frame marker is a single bit or a short pattern of bits that the transmitter injects periodically into the data stream. The receiver, having achieved data synchronization, correlates the known pattern with the incoming data stream at the known injection interval.

The advantage of the frame marker is its simplicity. Even a single bit can suffice as a frame marker if a sufficient number of correlations are accumulated before deciding whether or not the system has achieved synchronization.

The major drawback is that the sufficient number may be very large and thus the expected time required to acquire synchronization would be long. Therefore, frame markers are most useful in systems that transmit data continuously, like may telephony and computer links.



5. Network synchronization

For systems using coherent modulation techniques, one direction communication such as most microwave links, land line links or fiber optics links, the synchronization architecture is performed at the receiver. For systems using noncoherent modulation techniques or that involves many user accessing a central communication node, such as many satellite communication systems, the synchronization is performed at a terminal transmitter. This means that the terminal transmitter parameters are modified to achieve synchronization rather than modifying the central nodes receiver parameters. This approach is used for time division multiple access (TDMA). In TDMA each user is allotted a segment of time in which to transmit its information. The terminal transmitter must be synchronized with the system in order for its transmitted burst data to arrive at the central node at the time when the node is prepared to receive the data.

Synchronization of the terminal transmitter also makes sense with n systems that combine signal processing at the central node with frequency division multiple access (FDMA). If the terminals precorrect their transmission to be synchronized with the central node, the node can use a fixed set of channel filters and a single timing reference for the processing of all channels. Otherwise, the node would require a separate time and frequency acquisition and tracking capability for each incoming channel .It seems clear that terminal transmitter synchronization is often more reasonable system approach to synchronizing network Transmitter synchronization procedures may be classified being either open loop or closed loop

5.1 Open loop network synchronization techniques

Do not depend on any measurement of the arriving signal parameters at the central node. The terminal precorrect its transmission based on stored knowledge of link parameters that have been provided by some external authority but many possible be modified by observations of a return signal from the central node. Open loop techniques depend on link parameters being accurately known The main advantages of the open loop methods are that acquisitions is fast the procedure can work without a return link and the amount of real time computation that is required is small. The disadvantages of the open loop methods are that they require knowledge of the required link parameters variation.

5.2 Closed loop network synchronization techniques

Involve measurements of the synchronization accuracy of the incoming transmission from the terminal upon that their arrival at the central node, and the return of the results of these measurements to the terminal via a return path.

Thus, closed loop methods require a return path that provides a response to the terminal's transmissions, the ability in the terminal to recognize the response for what it is, and the ability in the terminal to modify the transmitter characteristics based on the response. The advantages of the closed loop are that no external source of knowledge is required for the system to work and the responses on the return link allow the system adapt easily and quickly to changing the characteristics. The disadvantages of closed loop methods are that they require a large amount of the real time processing and require two way links to every terminal.

6. Tracking and Acquisition in spread spectrum system

- Spread spectrum techniques are essentially synchronous. The Pseudo Noise sequences generated at the receiver must be phase locked with PN sequence used in transmitter and the synchronization of spread spectrum will be considered in two parts, Acquisition and Tracking.
- Usually the problem of timing acquisition is solved via a two-step approach:
  - *Initial code acquisition (coarse acquisition or coarse synchronization)* which synchronizes the transmitter and receiver to within an uncertainty of T_c.
  - *Code tracking* which performs and maintains fine synchronization between the transmitter and receiver.
- Acquisition means initial synchronization of spread spectrum. It is also called course

synchronization.

- Tracking starts after acquisition. It maintains the PN generator at the receiver in synchronous with the transmitter. It is also called fine synchronization.

6.1 Acquisition in spread spectrum system :

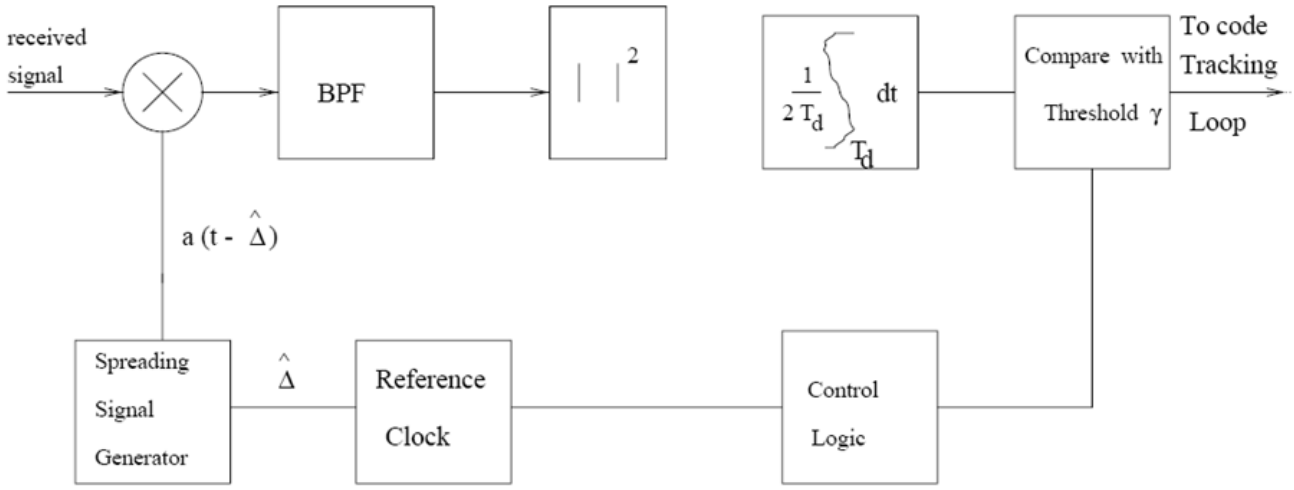
- Given the initial acquisition, code tracking is a relatively easy task and is usually accomplished by a delay lock loop (DLL).
- If the channel changes abruptly, the delay lock loop will lose track of the correct timing and initial acquisition will be re-performed.
- Compared to code tracking, initial code acquisition in a spread spectrum system is usually very difficult.

Acquisition techniques

- Serial search
- Parallel Search

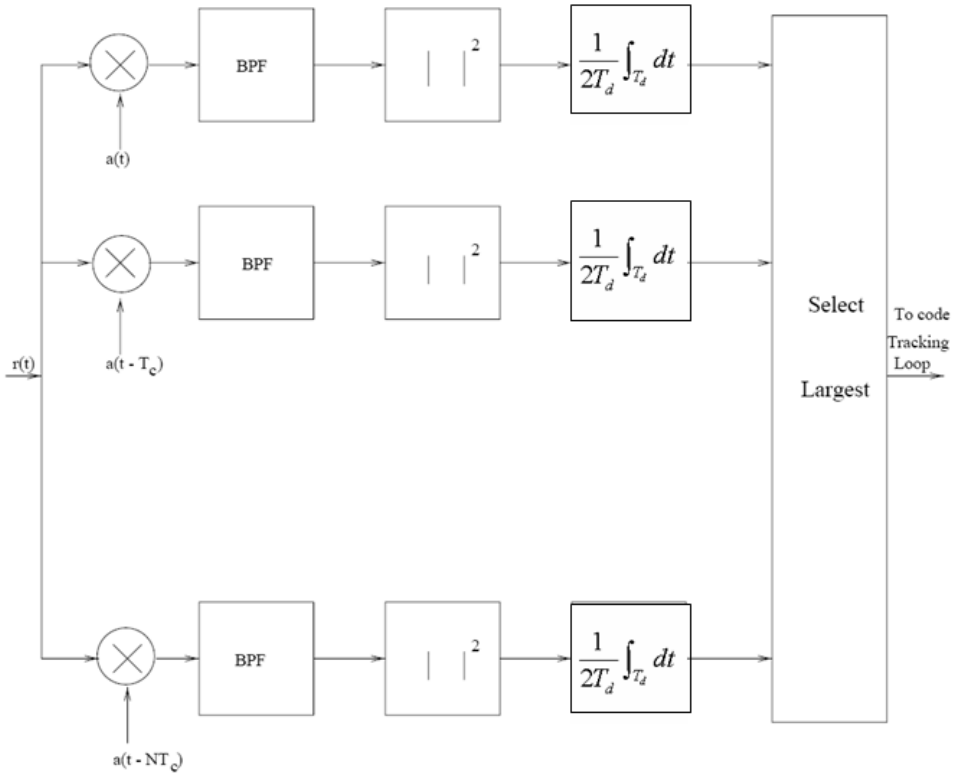
6.2 Serial search

- In this method, the acquisition circuit attempts to cycle through and test all possible phases one by one (serially) as shown in Figure
- The circuit complexity for serial search is low.
- However, penalty time associated with a miss is large.
- Therefore we need to select a larger integration (dwell) time to reduce the miss probability.
- This, together with the serial searching nature, gives a large overall acquisition time (i.e., slow acquisition).
- The received signal is correlated with the generated PN sequence. This cross-correlation is performed over the time interval of NTc.
- The output of the correlator is compared with a threshold. If it exceeds the threshold, then the required signal is obtained.
- If the threshold is not exceeded, them the PN generator output is advanced by half chip duration (1/2 Tc) and the correlation is performed.
- The output of the correlator is again compared with the threshold and the procedure is repeated.



6.3 Parallel search

- Unlike serial search, all the possible phases are tested simultaneously in the parallel search strategy as shown in Figure
- Obviously, the circuit complexity of the parallel search is high. The overall acquisition time is much smaller than that of the serial search.



The presence of noise causes two different kinds of errors in the acquisition process:

- A *false alarm* occurs when the integrator output exceeds the threshold for an incorrect hypothesized phase.
- A *miss* occurs when the integrator output falls below the threshold for a correct hypothesized phase.
- A false alarm will cause an incorrect phase to be passed to the code tracking loop which, as a result, will not be able to lock on to the DS-SS signal and will return the control back to the acquisition circuitry eventually.
- However, this process will impose severe time penalty to the overall acquisition time.
- On the other hand, a miss will cause the acquisition circuitry to neglect the current correct hypothesized phase.
- Therefore a correct acquisition will not be achieved until the next correct hypothesized phase comes around.
- The time penalty of a miss depends on acquisition strategy.

7. Tracking Techniques

- Matched filter energy detector
- Radiometer

7.1 Matched filter energy detector

The name is because the combination of the despreader and the integrator is basically an implementation of the matched filter for the spreading signal. It is based on the following basic working principle depicted in the Figure.

- The receiver hypothesizes a phase of the spreading sequence and attempts to despread the received signal using the hypothesized phase.
- If the hypothesized phase matches the sequence in the received signal, the wide-band spread spectrum signal will be despread correctly to give a narrowband data signal.
- Then a bandpass filter, with a bandwidth similar to that of the narrowband data signal, can be employed to collect the power of the despread signal.

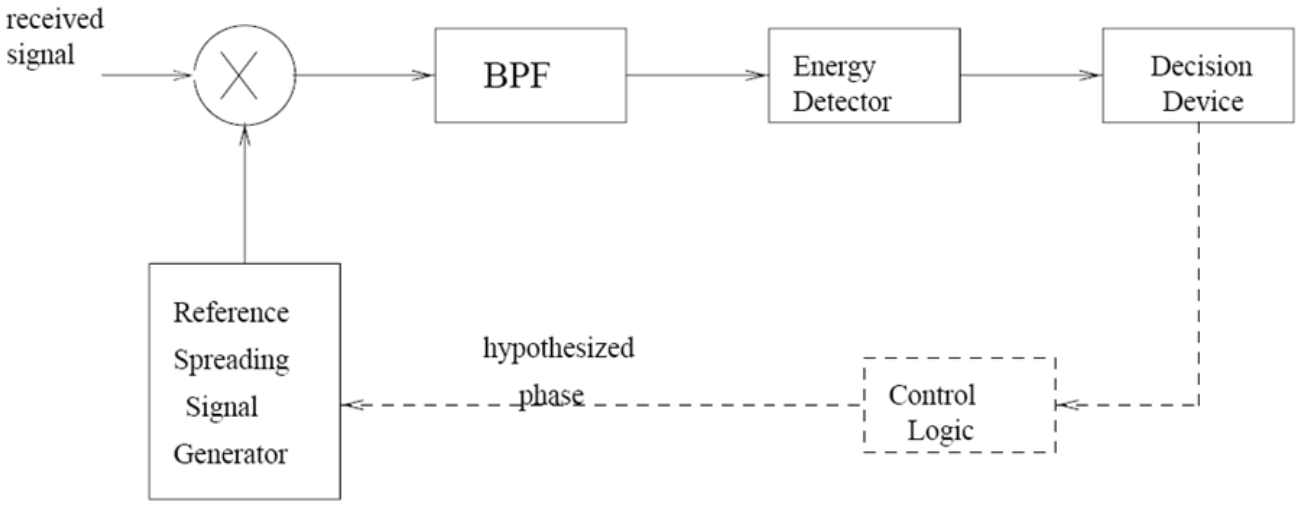


Figure. Generic Acquisition circuit

- Since the hypothesized phase matches the received signal, the BPF will collect all the power of the despread signal.
- In this case, the receiver decides a coarse synchronization has been achieved and activates the tracking loop to perform fine synchronization.
- On the other hand, if the hypothesized phase does not match the received signal, the despreader will give a wideband output and the BPF will only be able to collect a small portion of the power of the despread signal.
- Based on this, the receiver decides this hypothesized phase is incorrect and other phases should be tried.

7.2 Radiometer

- As before, the receiver hypothesizes a phase of the spreading process.
- The despread signal is bandpass filtered with a bandwidth roughly equal to that of the narrowband data signal.
- The output of the bandpass filter is squared and integrated for a duration of T_d to detect the energy of the despread signal.

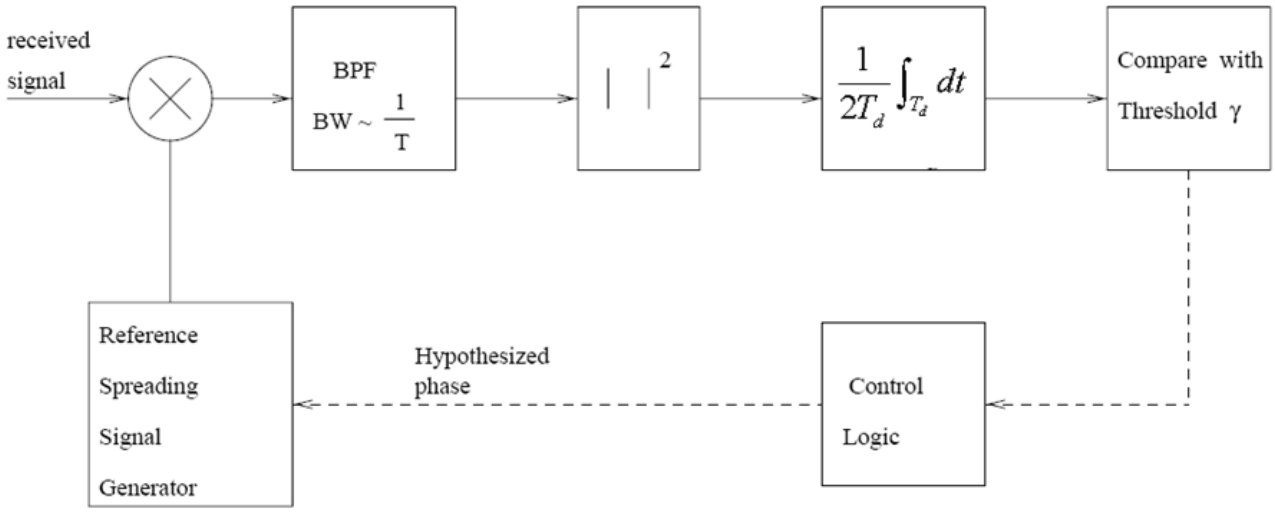


Figure. Acquisition circuit using radio meter

- The comparison between the matched filter energy detector and the radiometer brings out several important design issues for initial code acquisition circuits.
- **Dwell time**
  - The time needed to evaluate a single hypothesized phase of the spreading sequence.
- Neglecting the processing time for the other components in the acquisition circuit, the dwell time for the matched filter energy detector and the radiometer are determined by the integration times of the respective integrators in the matched filter energy detector and the radiometer.

- From the discussion above, the *dwell times* for the matched filter energy detector and the radiometer are T and T_d, respectively.
- In practice, we would like the dwell time to be as small as possible.
- For the matched filter energy detector, we cannot significantly reduce the integration time since the spreading sequence is usually designed to have a small out-of-phase autocorrelation magnitude, but the out-of-phase partial autocorrelation magnitude is not guaranteed to be small in standard sequence design methods.
- If we reduce the integration time significantly, the decision statistic would not be a function of the autocorrelation function, but rather a function of the partial autocorrelation function of the spreading sequence.
- Hence it would be difficult to distinguish whether or not we have a match between the hypothesized phase and the received signal, when noise is present.

- On the other hand, since the radiometer uses the BPF directly to detect whether there is a match or not and the integrator is simply employed to collect energy, we do not need to integrate for the whole period of the sequence as long as we have enough energy.
- The integration time and hence the dwell time can be smaller than *T*, provided that the BPF can settle to its steady state output in a much shorter duration than *T*
- Another design issue, which is neglected in the simplified example before, is the effect of noise.

PART A (2 Marks)

1. What are the three broad types of synchronization?
2. What is carrier synchronization?
3. List out methods for carrier synchronization?
4. What it is called symbol or bit synchronization?
5. What are the two methods used in bit and symbol synchronization?
6. What are the disadvantages of closed loop bit synchronization?
7. Define frame synchronization?
8. Why synchronization is required?
9. Define dwell time.
10. Differentiate tracking and acquisition.

PART B (12 Marks)

1. How PLL is used to achieve the Synchronization.
2. Explain in detailed about suppressed carrier loops and Costas loop
3. What is Symbol synchronization and explain it.
4. Explain briefly about early late gate synchronization.
5. Draw the block diagram for tracking and acquisition of spread spectrum and explain it