UNIT 4

SYLLABUS

UNIT 4 PLL AND TIMER CIRCUITS 9 Hrs.

Phase Locked Loop IC 565- Block schematic - Applications of PLL: FM demodulator and Frequency synthesizer-FSK Demodulator- VCO IC LM 566 - Timer IC LM 555 and its applications: Astable and Monostable multivibrator.

TABLE OF TOPICS

4.1 Phase Locked Loop (PLL)

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase- locked loop (PLL) came into vogue in the 1930 when it was used for radar synchronization and communication applications. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

Basic Principles

The basic block schematic of the PLL is shown in Fig. 4.1.1. This feedback system consists of Phase detector/comparator, low pass filter, error amplifier and Voltage Controlled Oscillator (VCO).

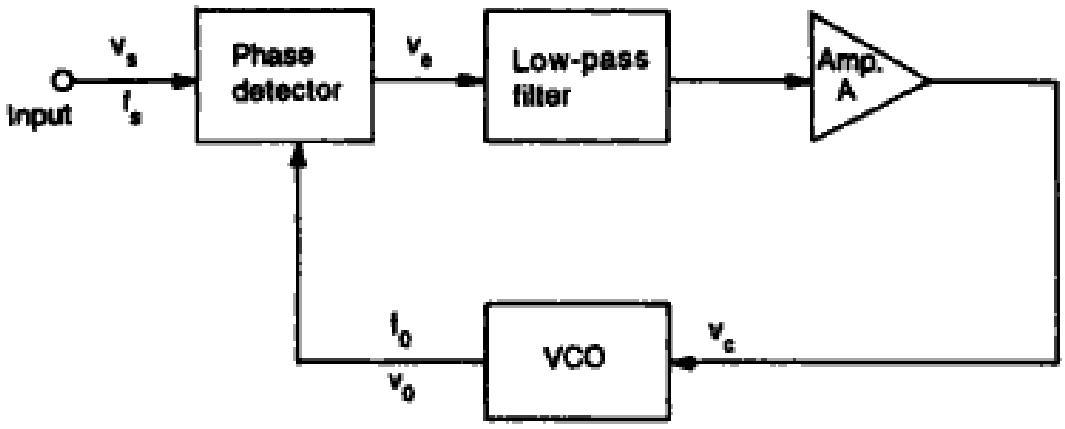

Fig. 4.1.1 Block schematic of the PLL

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and /or phase, an error voltage v_e is generated.

The phase detector is basically a multiplier and produces the sum (f_s+f_o) and difference (f_s-f_o) components at its output. The high frequency component (f_s+f_o) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage v_c to VCO.The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o.

Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal.

Thus, a PLL goes through three stages (i) free running (ii) capture and (iii) locked or tracking.

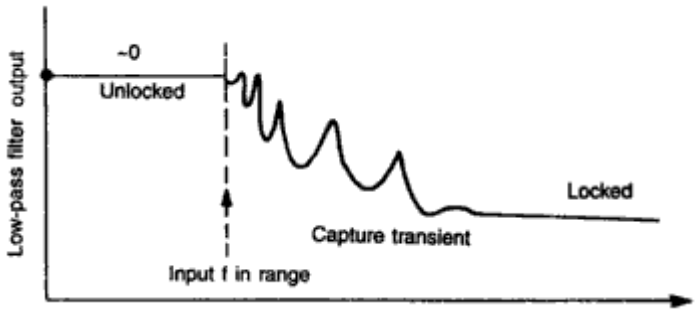

Fig. 4.1.2.The capture transient

Figure 4.1.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large de component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Lock-in Range

Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

Capture Range

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

Pull-in. time

The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

4.2. Phase Locked Loop IC 565

IC565 is available as a 14 pin DIP package and as 10 pin metal can package. The pin configuration and the block diagram are shown in Fig.4.2.1 (a, b). The output frequency of the VCO (both inputs 2, 3 grounded) is given by

$$f_o = \frac{0.25}{R_1 C_T} \text{ Hz}$$

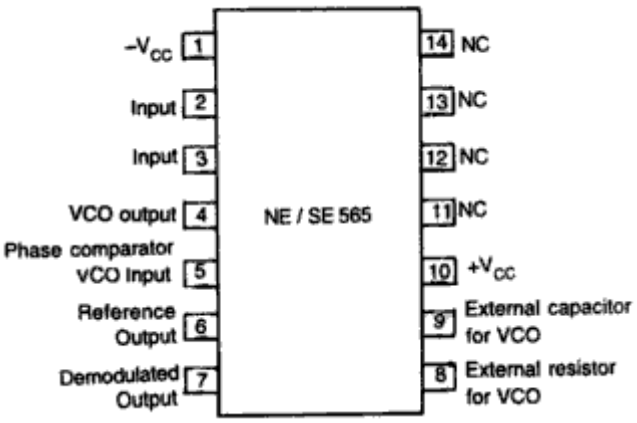

Fig. 4.2.1(a) Pin diagram

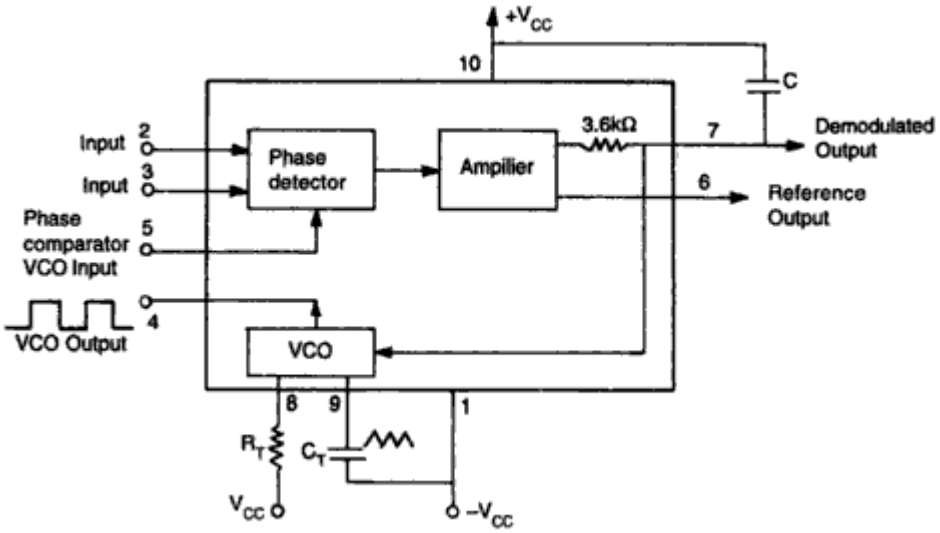

Fig. 4.2.1 (b) NE/SE565 PLL block diagram

Where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 KΩ and 20KΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 KΩ.

The important electrical parameters of 565 PLL are:

Operating frequency range : 0.001 Hz to 500 KHz

Operating voltage range	:	±6V to ±12V
Input level	:	10 mV rms min. to 3V pp max.
Input impedance		10 KΩ
Triangle wave amplitude	:	$2.4V_{pp}$ at ±6V supply voltage
Square wave amplitude	:	$5.4V_{pp}$ at ±6V supply voltage

4.3 Applications of PLL

The output from a PLL system can be obtained either as the voltage signal $v_C(t)$ corresponding to the error voltage in the feedback loop or as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application whereas the frequency output is used in signal conditioning frequency synthesis or clock recovery applications.

4.3.1 FM demodulator

The PLL can be very easily used as an FM detector or demodulator. Fig 4.3.1 shows the block diagram of FM detector.

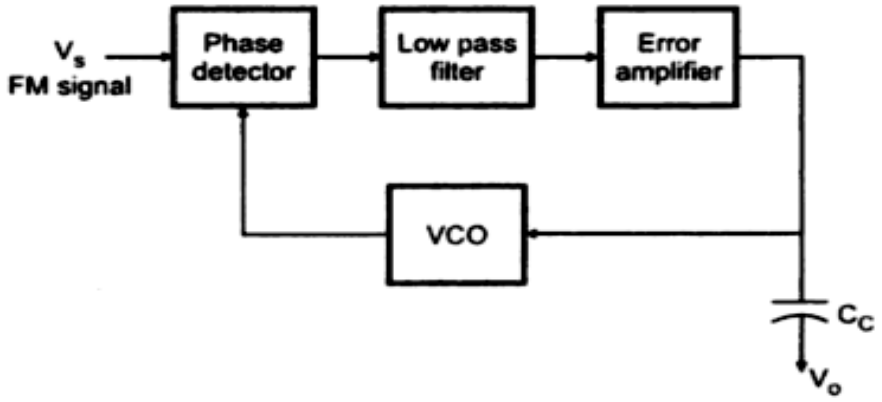

Fig.4.3.1 PLL as a FM Demodulator

When the PLL is locked in on the FM signal the VCO frequency follows the instantaneous frequency of the FM signal and the error voltage or VCO control voltage is proportional to the deviation of the input frequency from center frequency. Therefore the ac component of error voltage or control voltage of VCO will represent a true replica of the modulating voltage that is applied to the FM carrier at the transmitter. The faithful reproduction of modulating voltage

depends on the linearity will represent a true replica of the modulating voltage depends on the linearity between the instantaneous frequency deviation and the control voltage of VCO. It is also important to note that the FM frequency deviation and modulating frequency should remain in the locking range of PLL to get the faithful replica of the modulating signal. If the product of the modulation frequency f_m and the frequency deviation exceeds the $(\Delta f_C)^2$, the VCO will not be able to follow the instantaneous frequency of the FM signal.

4.3.2 Frequency synthesizer

The PLL can be used as the basis for the frequency synthesizer that can produce a precise series of frequencies that are derived from a stable crystal controlled oscillator. Fig. 4.3.2 shows the block diagram of frequency synthesizer. It is similar to frequency multiplier circuit except that divided by M network is added at the input of phase lock loop. The frequency of the crystal-controlled oscillator is divided by an integer factor M by divider network to produce a frequency f_{osc}/M, where f_{osc} is the frequency of the crystal controlled oscillator. The VCO frequency f_{vco} is similarly divided by factor N by divider network to give frequency equal to f_{vco}/N. when the PLL is licked in on the divided-down oscillator frequency we will have $f_{osc}/M = f_{vco}/N$, so that $f_{vco} = f_{osc}N/M$).

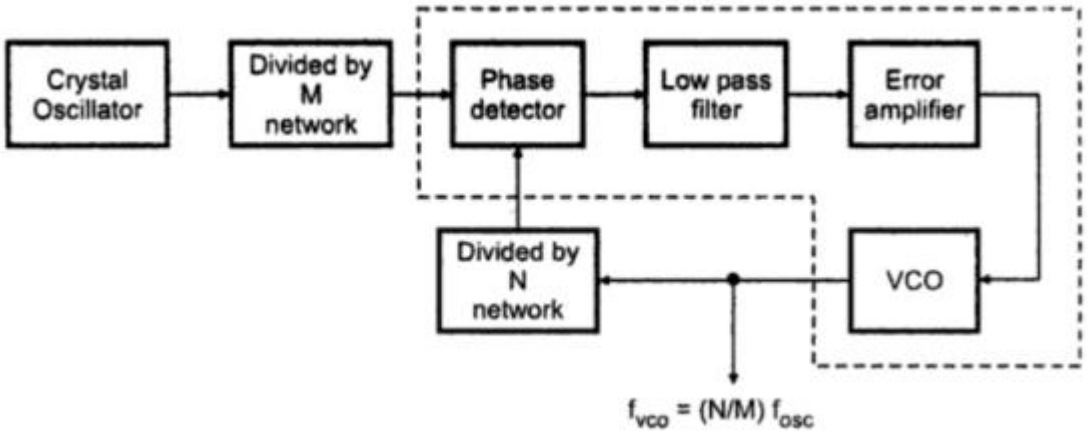

Fig. 4.3.2 Block diagram of Frequency synthesizer

By adjusting divider counts to desired values large number of frequencies can be produced, all derived from the crystal controlled oscillator.

4.4 VCO IC LM 566

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 5.8(a, b). Referring to Fig. 5.8 (b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

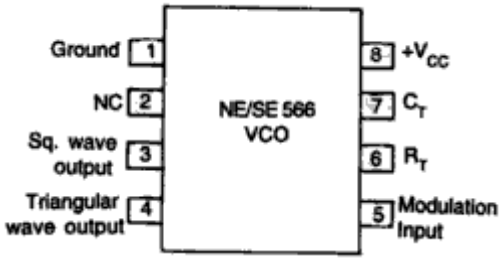

Fig. 5.8 (a) Pin configuration of VCO

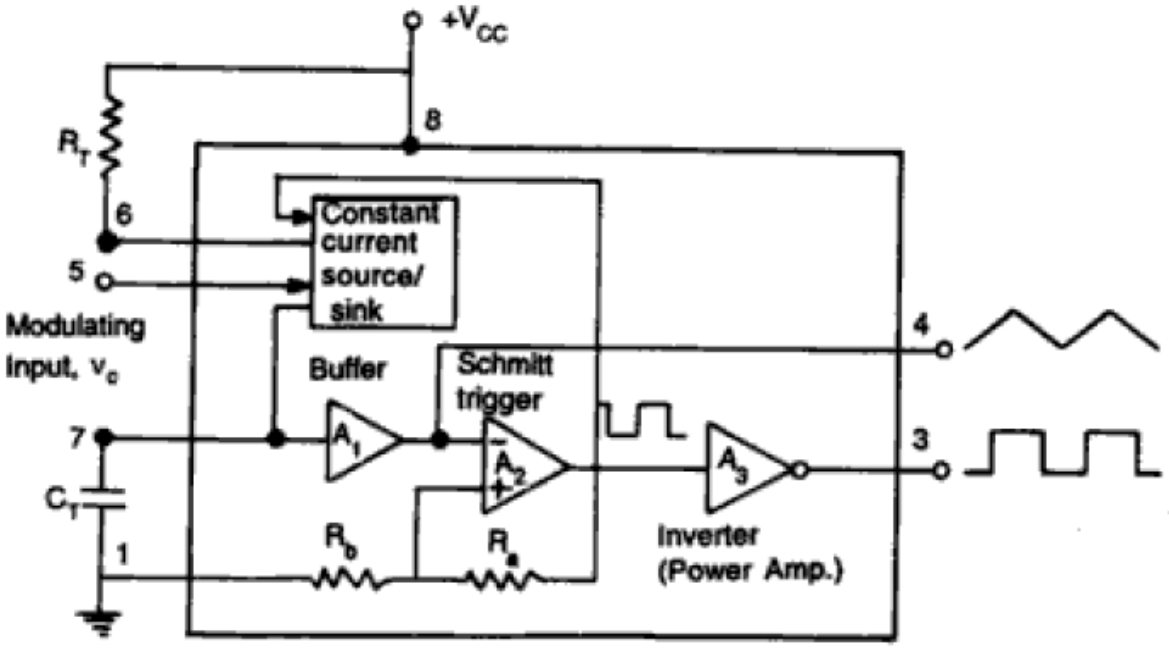

Fig. 5.8 (b) Block Diagram of VCO

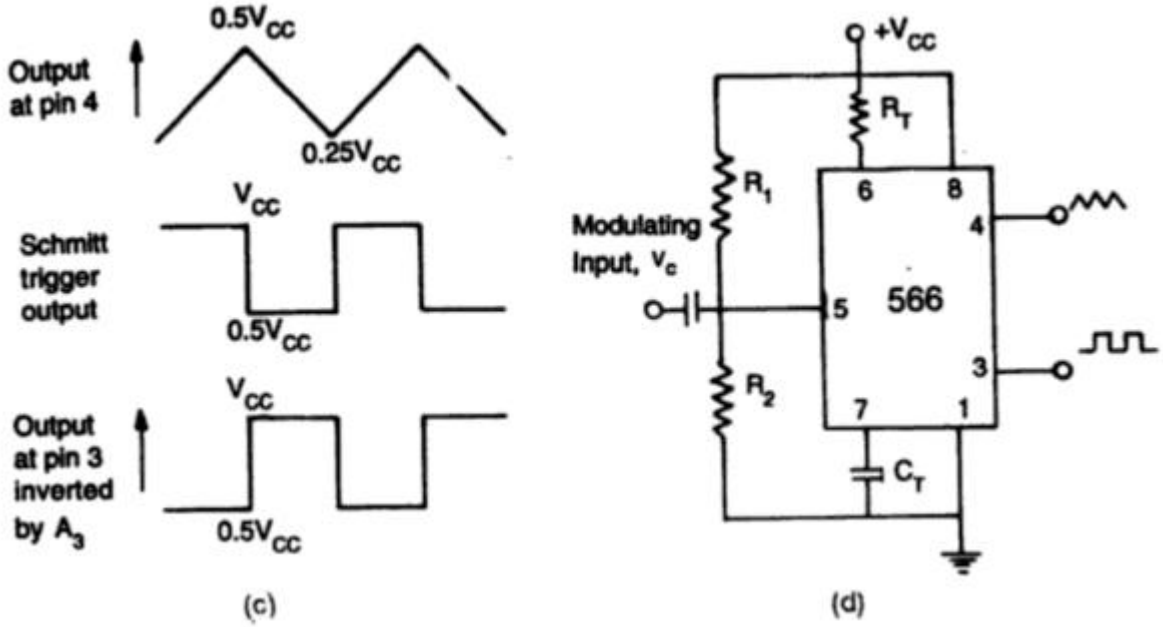

Fig. 5.8 (c) Output Waveform (d) Typical connection

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{cc} to 0.25 V_{cc}. In Fig. 5.8 (c), when the voltage on the capacitor C_T exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The output waveforms are shown in Fig. 5.8 (c).

The output frequency of the VCO can be calculated as follows:

The total voltage on the capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta v = 0.25\ V_{cc}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or,
$$\frac{0.25\ V_{cc}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\ V_{cc} C_T}{i}$$

The time period T of the triangular waveform = $2\Delta t$. The frequency of oscillator f_o is,

$$f_o = \frac{1}{T} = \frac{1}{2\ \Delta t}$$

$$= \frac{i}{0.5\ V_{cc} C_T}$$

But,
$$i = \frac{V_{cc} - v_c}{R_T}$$

where, v_c is the voltage at pin 5. Therefore,

$$f_o = \frac{2(V_{cc} - v_c)}{C_T R_T V_{cc}}$$

The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit as shown in Fig. 5.8 (d). The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{cc} to V_{cc} which can produce a frequency variation of about 10 to 1. With no modulating input signal, if the voltage at pin 5 is biased† at (7/8) V_{cc}, Eq. gives the VCO output frequency as,

$$f_o = \frac{2(V_{cc} - (7/8)\ V_{cc})}{C_T R_T V_{cc}} = \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T}$$

4.5 Timer IC LM 555

The various features of the IC 555 timer are :

1. The 555 is a monolithic timer device which can be used to produce accurate and highly stable time delays or oscillation. It can be used to produce time delays ranging from few microseconds to several hours.
2. It has two basic operating modes : monostable and astable
3. It is available in three packages : 8-pin metalcan, 8-pin mini DIP or a 14-pin DIP. A 14-pin package is IC 556 which consists of two 555 timers.
4. The NE 555 (Signetics) can operate with a supply voltage in the range of 4.5 V to 18V and is capable of sourcing and sinking output currents of 200 mA. Its CMOS version (TLC 555) can operate over a supply range of 2V to 18V and has output current sinking and sourcing capabilities of 100 mA and 10mA, respectively.
5. It has a very high temperature stability, as it is designed to operate in the temperature range of –55° to 125° C.
6. Its output is capatible with TTL, CMOS and Op-Amp circuits.

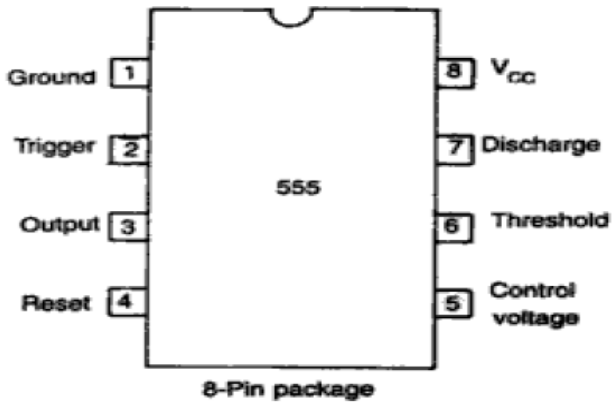

Fig. 5.9 Pin Diagram of IC 555

Functional description of IC 555

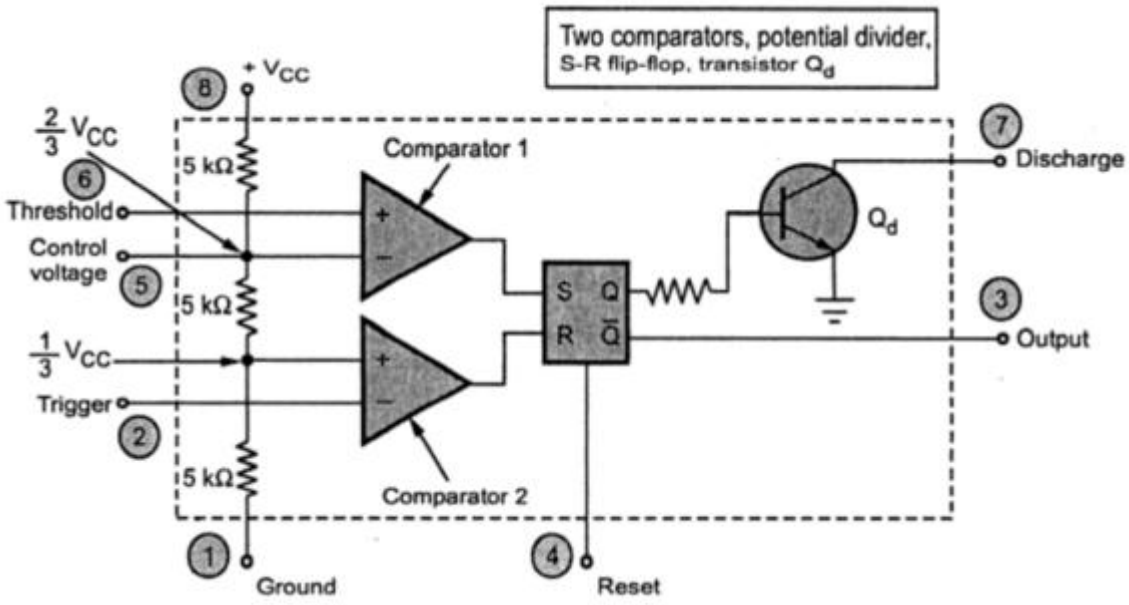

Fig. 5.10 Functional Diagram of IC 555

Pin 1 : Ground

All the voltages are measured with respect to this terminal.

Pin 2 : Trigger

The IC 555 uses two comparators. The voltage divider consists of three equal resistances. Due to voltage divider, the voltage of noninverting terminal of comparator 2 is fixed at V_{CC} / 3. The inverting input of comparator 2 which is compared with $V_{CC}/3$, is nothing but trigger input brought out as pin number 2. When the trigger input is slightly less than V_{CC} /3 the comparator 2 output goes high. This output is given to reset input of R-S flip-flop. So high output of comparator 2 resets the flip-flop.

Pin 3 : Output

The complementary signal output ($\bar{Q}$) of the flip-flop goes to pin 3 which is the output. The load can be connected in two ways. One between pin 3 and ground while other between pin 3 and pin 8.

Pin 4 : Reset

This is an interrupt to the timing device. When pin 4 is grounded, it stops the working of device and makes it off. Thus, pin 4 provides on/off feature to the IC 555. This reset input overrides all other functions within the timer when it is momentarily grounded.

Pin 5 : Control Voltage Input

In most of the applications, external control voltage input is not used. This pin is nothing but the inverting input terminal of comparator 1. The voltage divider holds the voltage of this input at $2/3\,V_{CC}$. This is reference level for comparator 1 with which threshold is compared. If reference level required is other than $2/3\ V_{CC}$ for comparator 1 then external input is to be given to pin 5.

If external input applied to pin 5 is alternating then the reference level for comparator 1 keeps on changing above and below $2/3\ V_{CC}$. Due to this, the variable pulse width output is possible. This is called **pulse width modulation,** which is possible due to pin 5.

Pin 6 : Threshold

This is the noninverting input terminal of comparator 1. The external voltage is applied to this pin 6. When this voltage is more than $2/3\ V_{CC}$, the comparator 1 output goes high. This is given to the set input of R-S flip-flop. Thus high output of comparator 1 sets the flip-flop. This makes Q of flip-flop high and $\overline{Q}$ low. Thus the output of IC 555 at pin 3 goes low.

Remember that output at pin 3 is $\overline{Q}$ which is complementary output of flip-flop. In short,

For threshold $> \frac{2}{3} V_{CC}$, flip-flop → set, Q → high, output at pin 3 → low

For trigger $< \frac{1}{3} V_{CC}$, flip-flop → reset, Q → low, output at pin 3 → high

Pin 7 : Discharge

This pin is connected to the collector of the discharge transistor Q_d. When the output is high then Q is low and transistor Q_d is off. It acts as an open circuit to the external capacitor C to be connected across it, so capacitor C can charge as described earlier. When output is low, Q is high which drives the base of Q_d high, driving transistor Q_d in saturation. It acts as short circuit, shorting the external capacitor C to be connected across it.

Pin 8 : Supply $+V_{CC}$

The IC 555 timer can work with any supply voltage between 4.5 V and 16 V.

4.5.2 Monostable Multivibrator

The IC 555 timer can be operated as a monostable multivibrator by connecting an external resistor and a capacitor as shown in the Fig. 5 .11.

The circuit has **only one stable state**. When trigger is applied, it produces a pulse at the output and returns back to its stable state. The duration of the pulse depends on the values of R and C. As it has only one stable state, it is called one shot multivibrator.

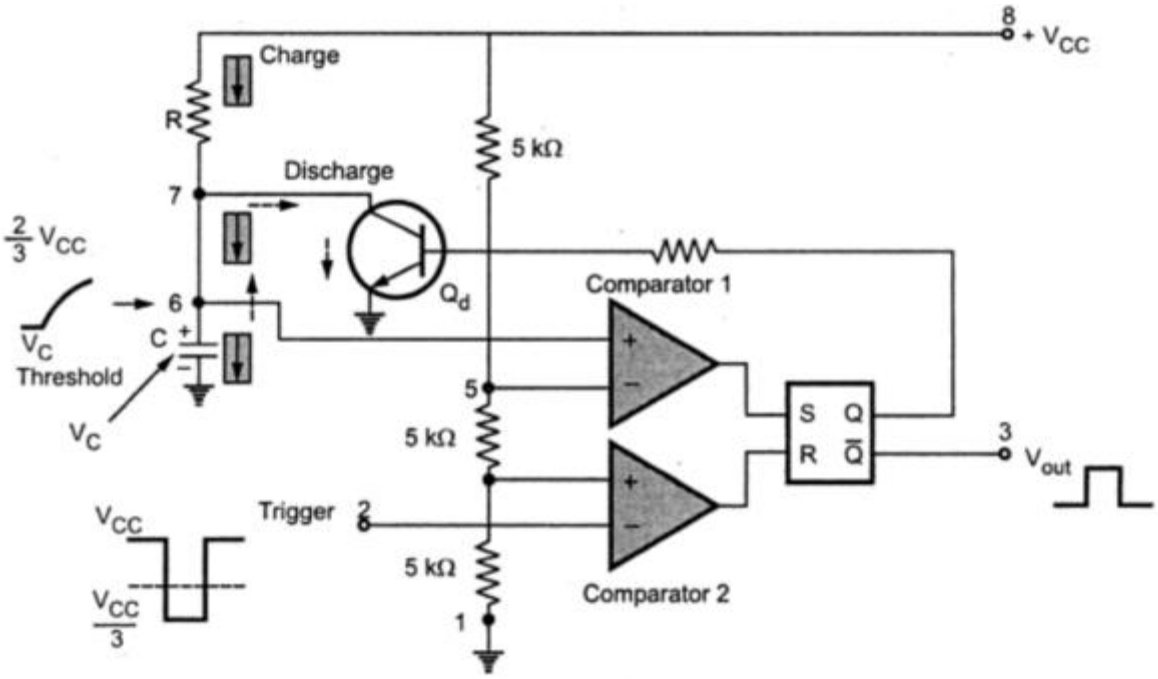

Fig. 5.11 Monostable Multivibrator

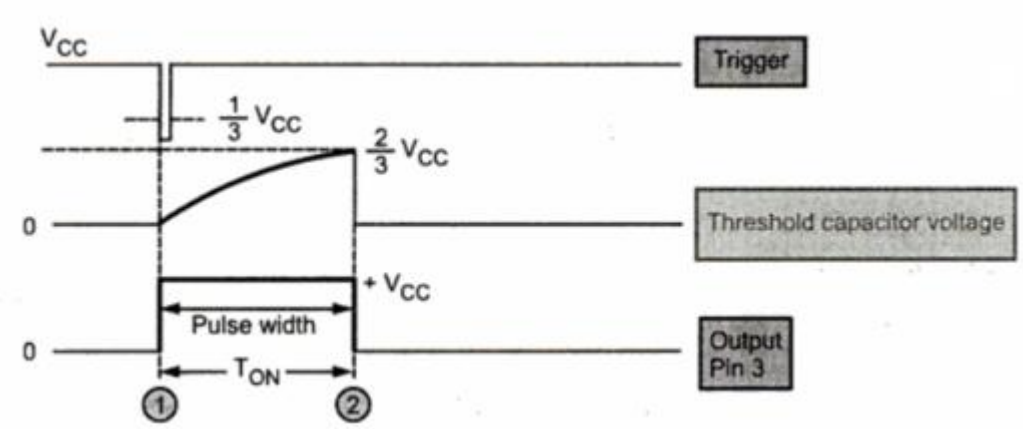

Fig. 5.12 Waveforms of monostable operation

Operation

The flip-flop is initially set i.e. Q is high. This drives the transistor Q_d in saturation. The capacitor discharges completely and voltage across it is nearly zero. The output at pin 3 is low.

When a trigger input, a low going pulse is applied, then circuit state remains unchanged till trigger voltage is greater than 1/3 V_{CC}. When it becomes less than 1/3 V_{CC}, then comparator 2 output goes high. This resets the flip-flop so Q goes low and $\bar{Q}$ goes high. Low Q makes the transistor Q_d off. Hence capacitor starts charging through resistance R, as shown by dark arrows in the Fig. 5.11.

The voltage across capacitor increases exponentially. This voltage is nothing but the threshold voltage at pin 6. When this voltage becomes more than 2/3 V_{CC} , then comparator 1 output goes high. This sets the flip-flop i.e. Q becomes high and $\overline{Q}$ low. This high Q drives the transistor Q_d in saturation. Thus capacitor C quickly discharges through Q_d as shown by dotted arrows in the Fig. 5 .12.

So it can be noted that V_{out} at pin 3 is low at start, when trigger is less than 1/3 V_{CC} it becomes high and when threshold is greater than 2/3 V_{CC} again becomes low, till next trigger pulse occurs. So a rectangular wave is produced at the output. The pulse width of this rectangular pulse is controlled by the charging time of capacitor. This depends on the time constant RC. **Thus RC controls the pulse width.** The waveforms are shown in the Fig. 5.12.

Derivation

The voltage across capacitor increases exponentially and is given by

$$V_C = V\left(1 - e^{-t/CR}\right)$$

If $V_C = 2/3\ V_{CC}$

then $$\frac{2}{3} V_{CC} = V_{CC}\left(1 - e^{-t/CR}\right)$$

$$\frac{2}{3} - 1 = -e^{-t/CR}$$

$$\frac{1}{3} = e^{-t/CR}$$

$$\therefore \quad -\frac{t}{CR} = -1.0986$$

$$\therefore \quad t = +1.0986\ CR$$

$$\therefore \quad t \approx 1.1\ CR$$

where C in farads, R in ohms, t in seconds.

Thus, we can say that voltage across capacitor will reach 2/3 V_{CC} in approximately 1.1 times, time constant i.e. 1.1 RC

Thus the pulse width denoted as W is given by,

$$\boxed{W = 1.1\ RC}$$

Applications of Monostable Multivibrator

- Missing pulse Detector
- Linear Ramp Generator
- Frequency Divider
- Pulse Width Modulation

Schematic diagram

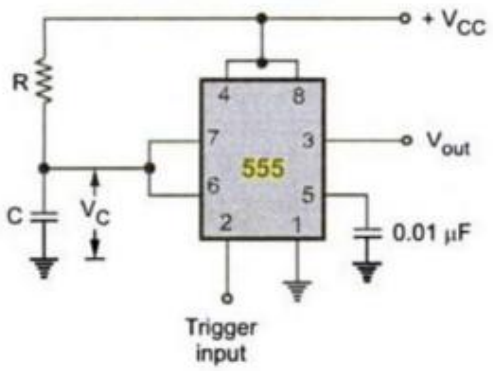

Fig. 5.13 555 timer as monostable multivibrator

Generally a schematic diagram of the IC 555 circuits is shown which does not include comparators, flip-flop etc. It only shows the external components to be connected to the 8 pins of IC 555. Thus, the schematic diagram of IC 555 as a monostable multivibrator is shown in the Fig. 5.13 .

The external components R and C are shown. To avoid accidental reset, pin 4 is connected to pin 8 which is supply $+V_{CC}$. To have the noise filtering of control voltage, the pin 5 is grounded through a small capacitor of 0.01 μF.

Example *Design a monostable multivibrator for a time delay of 1 second using the IC 555.*

Solution :

$W = 1$ sec.

But $W = 1.1\ RC$ i.e. $1.1\ RC = 1$

$\therefore\ RC = 0.90909$

Choose $C = 10\ \mu F$

$$\therefore\ R = \frac{0.90909}{10 \times 10^{-6}} = 90.909\ k\Omega \approx 91\ k\Omega$$

Pulse Width Modulation (PWM)

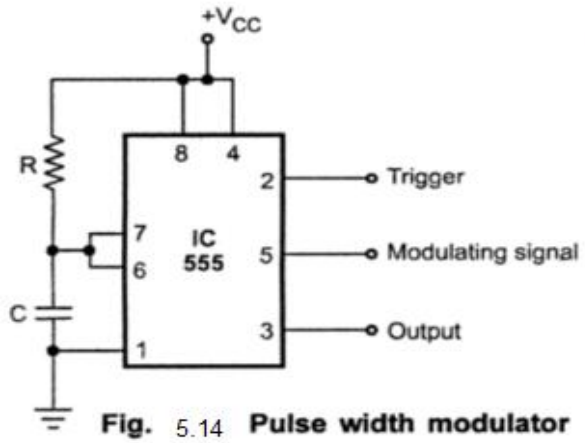

Fig. 5.14 Pulse width modulator

The Fig. 5.14 shows pulse width modulator. It is basically a monostable multivibrator with a modulating input signal applied at the control voltage input (pin 5). Internally, the control voltage is adjusted to the 2/3 V_{CC}. Externally applied modulating signal changes the control voltage, and hence the threshold voltage level of the upper comparator (comparator 1). As a result, time period required to charge the capacitor upto threshold voltage level changes, giving pulse width modulated signal at the output as shown in the Fig. 5.15 .

It may be noted from the output waveform that the pulse duration varies according to the modulating signal level, but the frequency of the output pulses is same as that of the trigger input signal.

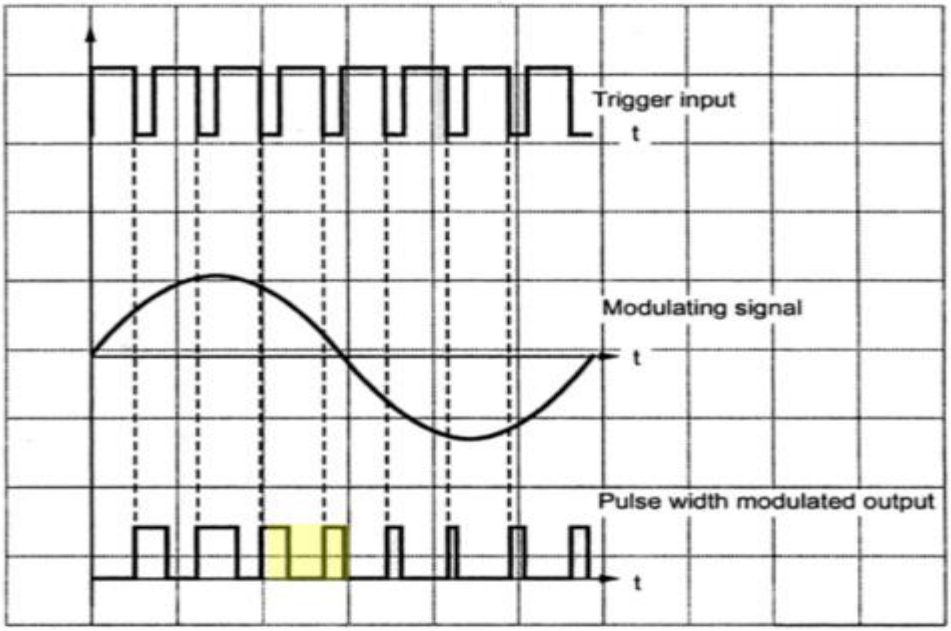

Fig. 5.15 Pulse Width Modulator Waveforms

4.5.3 Astable Multivibrator

The Fig. 5.16 shows the IC 555 connected as an astable multivibrator. The threshold input is connected to the trigger input. Two external resistances R_A, R_B and a capacitor C is used in the circuit.

This circuit has no stable state. The circuits changes its state alternately. Hence the operation is also called free running nonsinusoidal oscillator.

Operation

When the flip-flop is set, Q is high which drives the transistor Q_d in saturation and the capacitor gets discharged. Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than 1/3 V_{CC}, comparator 2 output goes high. This resets the flip-flop hence Q goes low and $\overline{Q}$ goes high.

The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and V_{CC}. The charging path is shown by thick arrows in the Fig. 5.16 . As total resistance in the charging path is $(R_A + R_B)$, the charging time constant is $(R_A + R_B)$ C.

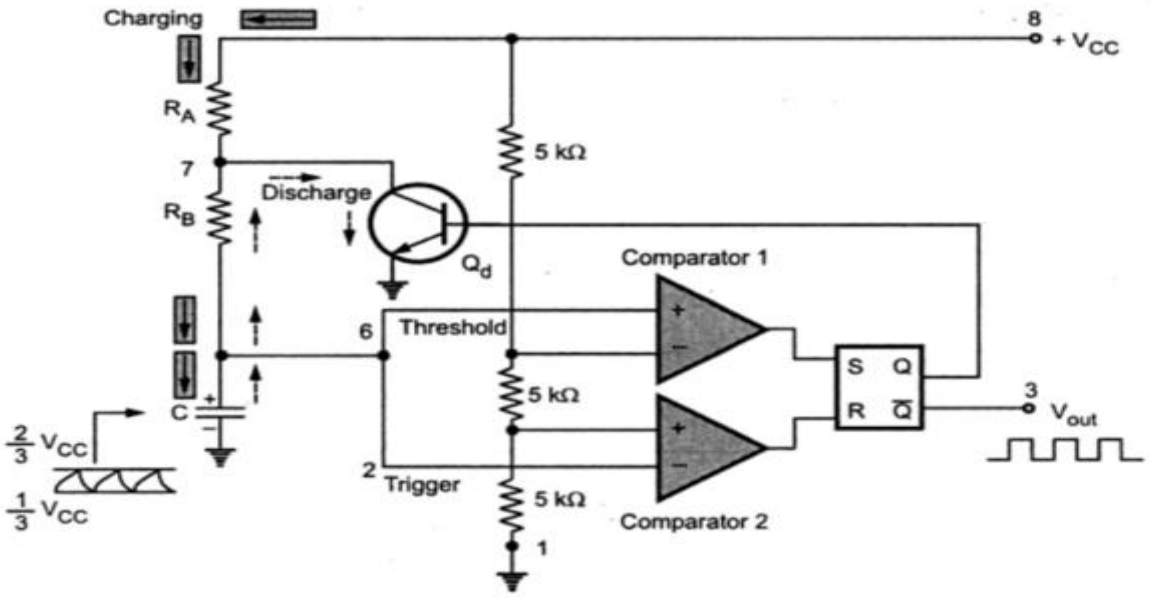

Fig. 5.16 Astable operation of IC 555

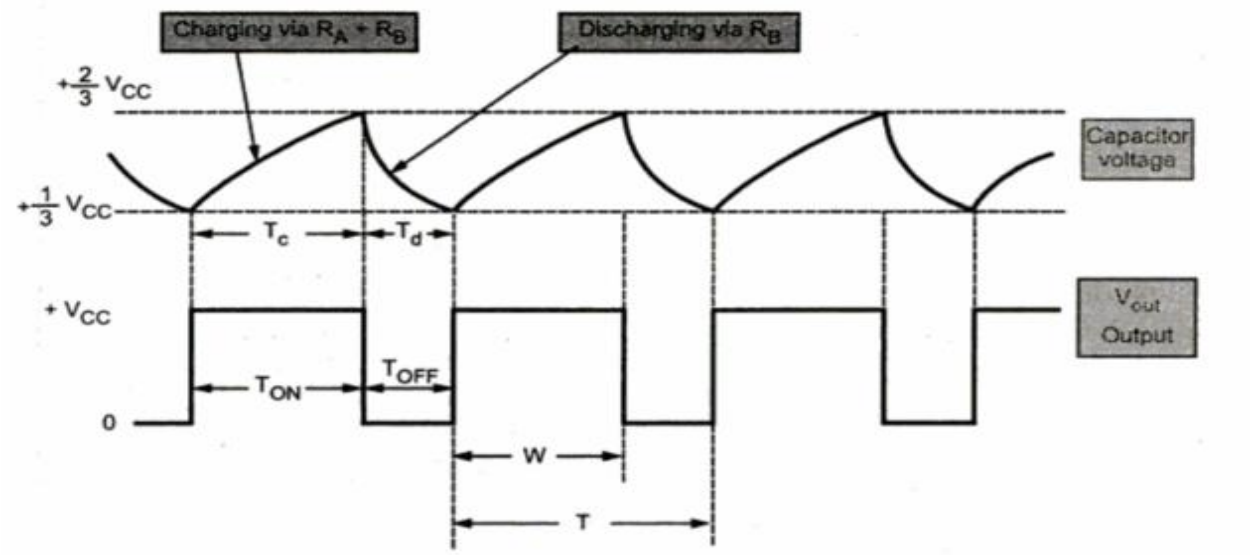

Fig.5.17 Waveforms of astable operation

Now the capacitor voltage is also a threshold voltage. While charging, capacitor voltage increases i.e. the threshold voltage increases. When it exceeds 2/3 V_{CC}, then the comparator 1 output goes high which sets the flip-flop. The flip-flop output Q becomes high and output at pin 3 i.e. $\overline{Q}$ becomes low. High Q drives transistor Q_d in saturation and capacitor starts discharging through resistance R_B and transistor Q_d. This path is shown by dotted arrows in the Fig. 5.16 . Thus the discharging time constant is R_B C. When capacitor voltage becomes less than 1/3 V_{CC}, comparator 2 output goes high, resetting the flip-flop. This cycle repeats.

Thus when capacitor is charging, output is high while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially rising and falling. The waveforms are shown in the Fig. 5.17 .

Duty Cycle

Generally the charging time constant is greater than the discharging time constant. Hence at the output, the waveform is not symmetric. The high output remains for longer period than low output. The ratio of high output period and low output period is given by a mathematical parameter called duty cycle. It is defined as the ratio of ON time i.e. high output to the total time of one cycle. As shown in the Fig. 5.17 .

W = time for output is high = T_{ON}

T = time of one cycle

$$\therefore \quad D = \text{duty cycle} = \frac{W}{T}$$

$$\therefore \quad \boxed{\%\ D = \frac{W}{T} \times 100\ \%}$$

The charging time for the capacitor is given by,

$$T_c = \text{Charging time} = 0.693\ (R_A + R_B)\ C$$

While the discharge time is given by,

$$T_d = \text{Discharging time} = 0.693\ R_B\ C$$

Hence the time for one cycle is,

$$T = T_c + T_d = 0.693\ (R_A + R_B)\ C + 0.693\ R_B\ C$$

$$\therefore \quad \boxed{T = 0.693\ (R_A + 2\ R_B)\ C}$$

while $W = T_c = 0.693\ (R_A + R_B)\ C$

$$\therefore \quad \%D = \frac{W}{T} \times 100 = \frac{0.693\ (R_A + R_B)\ C}{0.693\ (R_A + 2\ R_B)\ C} \times 100$$

$$\therefore \quad \boxed{\%\ D = \frac{(R_A + R_B)}{(R_A + 2\ R_B)} \times 100}$$

While the frequency of oscillations is given by,

$$f = \frac{1}{T} = \frac{1}{0.693(R_A + 2\ R_B)C}$$

$$\therefore \quad \boxed{f = \frac{1.44}{(R_A + 2\ R_B)C}\ \text{Hz}}$$

If R_A is much smaller than R_B, duty cycle approaches to 50% and output waveform approaches to square wave.

Schematic Diagram

The Fig. 5.18 shows the schematic diagram of astable timer circuit. It shows only the external components R_A, R_B and C. The pin 4 is tied to pin 8 and pin 5 is grounded through a small capacitor.

The important application of astable multivibrator is voltage controlled oscillator (VCO).

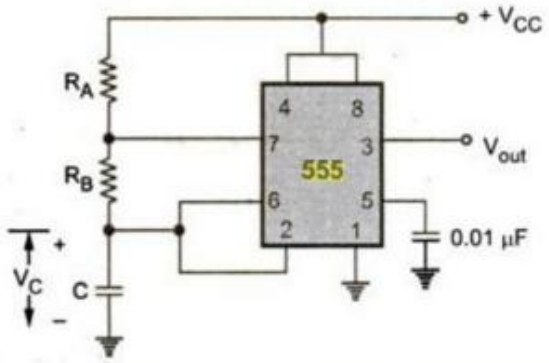

Fig. 5.18 555 timer as astable multivibrator

Applications of astable multivibrator

- Square wave generator
- Voltage controlled oscillator
- FSK Generator

Example:

A 555 timer is configured to run in astable mode with R_A = 4KΩ, R_B = 4KΩ and C=0.01μF. Determine the frequency of the output and duty cycle.

Solution:

The frequency of the output is given by,

$$f = \frac{1.44}{(R_A + 2R_B)C}$$

$$f = \frac{1.44}{((4 + 2 \times 4) \times 10^3 \times 0.01 \times 10^{-6})}$$

$$f = 12\ KHz$$

The duty cycle is given by,

$$D = \frac{R_A + R_B}{R_A + 2R_B}$$

$$D = \frac{4 + 4}{4 + (2 \times 4)} \times 100$$

$$D = 0.6667 \times 100$$

$$D = 66.67\%$$

Thus the duty cycle is 66.67%

Comparison of Monostable and astable multivibrator

S. No.	Monostable multivibrator	Astable multivibrator
1.	It has only one stable state and one quasi stable state	There is no stable state at all
2.	Trigger is required for the operation change its state from stable to quasi stable state	No trigger is required for change of state. Thus called *free-running*.
3.	Two components R and C are necessary with IC555.	Three components R_A, R_B and C are necessary with IC555.
4.	The pulse width of quasi-stable state is given by, *W=1.1 RC* seconds	The frequency is given by, *f=1.44/ (R_A+2R_B) Hz*
5.	The frequency of operation is controlled by frequency of trigger pulse applied.	The frequency of operation is controlled by R_A, R_B and C.
6.	The applications are, timer, frequency divider, pulse width modulation etc.	The applications are, square wave generator, flasher VCO, FSK generator etc.