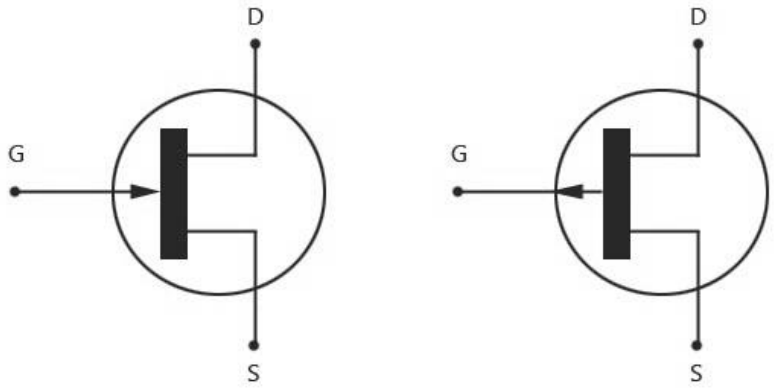
UNIT 3 FIELD EFFECT TRANSISTOR

JFET

JFET is a unipolar-transistor, which acts as a voltage controlled current device and is a device in which current at two electrodes is controlled by the action of an electric field at a p-n junction.

A JFET, or junction field-effect transistor, or JUGFET, is a FET in which the gate is created by reverse-biased junction (as opposed to the MOSFET which creates a junction via a field generated by conductive gate, separated from the gate region by a thin insulator).

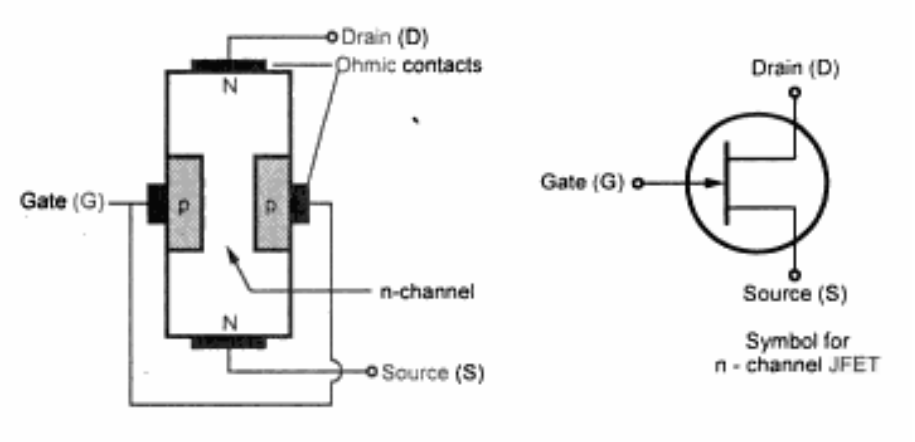


JFET-N-Channel and P-channel Schematic Symbol

Construction

n-channel JFET

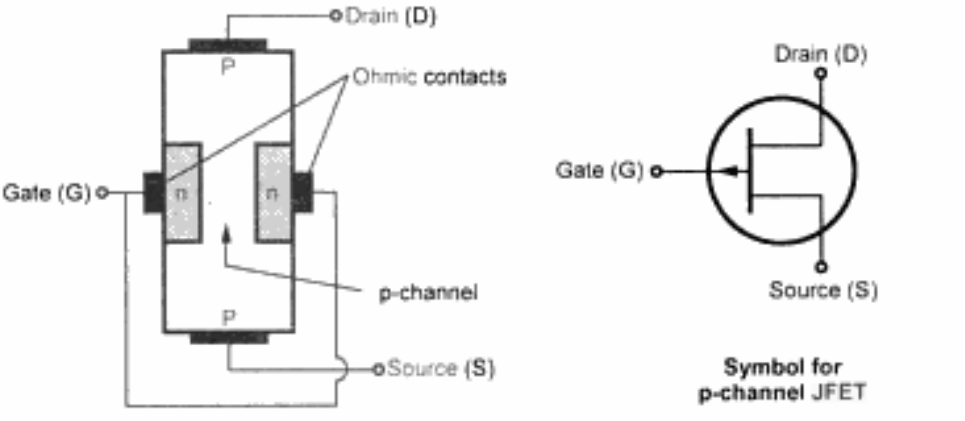
The figure shows construction and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and its two ends, two ohmic contacts are made which is the drain and source terminals of FET. Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the channel. Since this channel is in the n type bar, the FET is known as n-channel JFET.



The electrons enter the channel through the terminal called source and leave through the terminal called drain. The terminals taken out from heavily doped electronics of p type material are called gates. These electrodes are connected together and only one terminal is taken out, which is called gate, as shown in the figure.

p-channel JFET

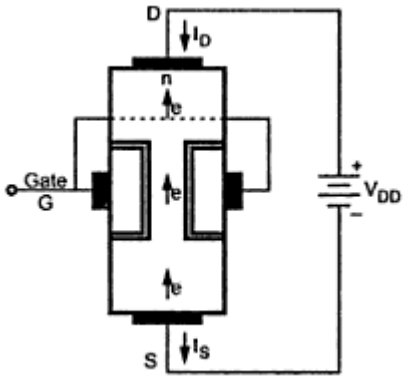
The device could be made of p type bar with two n type gates as shown in the figure. This will be p-channel JFET. The principle of working of n-channel JFET and p-channel JFET are similar. The only difference being that in n-channel JFET the current is carried by electrons while in p-channel JFET, it is carried by holes.



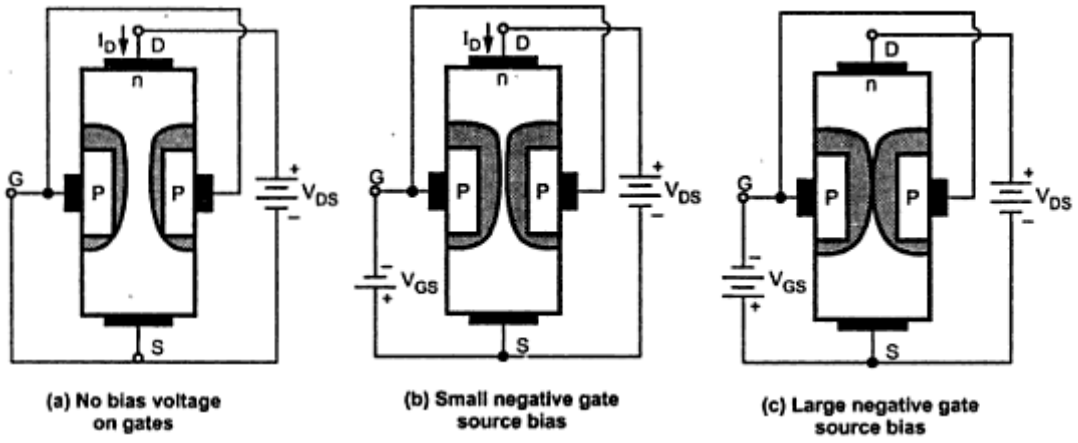
Operation

In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero. The gate current in JFET is often neglected and assumed to be zero.

Let us consider the circuit in the figure, voltage V_{DD} is applied between drain and source. Gate terminal is kept open. The bar is of n-type material. Due to the polarities of applied voltage as shown in the fig, the majority carriers i.e. the electrons start flowing from the source to the drain. The flow of electrons makes the drain current, $I_{D.}$



The majority carriers move from source to drain through the space between the gate regions. The space is commonly known as **channel.** The width of this channel can be controlled by varying the gate voltage. To see the effect of gate voltage on channel-width and on drain current $I_{D,}$ consider the diagram below.



(a) No bias voltage on gates

(b) Small negative gate source bias

(c) Large negative gate source bias

The figure (a) shows that an n-channel JFET with the gate directly connected to the source terminal. When drain voltage V_{DS} is applied, a drain current I_D flows in the direction shown. Since the n-material is resistive, the drain current causes a voltage drop along the channel. This voltage drop reverse biases the pn junctions, and causes the depletion regions to penetrate into the channel. Since gate is heavily doped and the channel is lightly doped the width of the depletion region will mainly be spread in the channel as shown in fig (a). This penetration depends on the reverse bias voltage. From

the fig it can be observed that depletion region width is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that reverse bias is not uniform near the junction as it gradually increases from source side to drain side.

The depletion region does not contain charge carriers. The space between two depletion regions is available for conducting portion of the channel. When reverse bias voltage is applied externally to the gate, the reverse bias will increase and hence increase the penetration of the depletion region which reduces the width of the conducting portion of the channel. When the width of the conducting portion of the channel reduces, the no. of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces.

When the external reverse bias voltage at the gate is increased as shown in fig (b) & (c) the depletion regions will increase more and at a particular stage the width of the depletion region will be equal to the original width of the depletion regions will increase more and more, and stage will come when the width of the depletion regions will be equal to the original width of the channel, leaving zero width for conducting portion of the channel, as shown in the fig (c). This will prevent any current flow from drain to source and this will cut off the drain current. The gate to source voltage that produces cutoff is known as cutoff voltage ($V_{GS\ (OFF)}$).

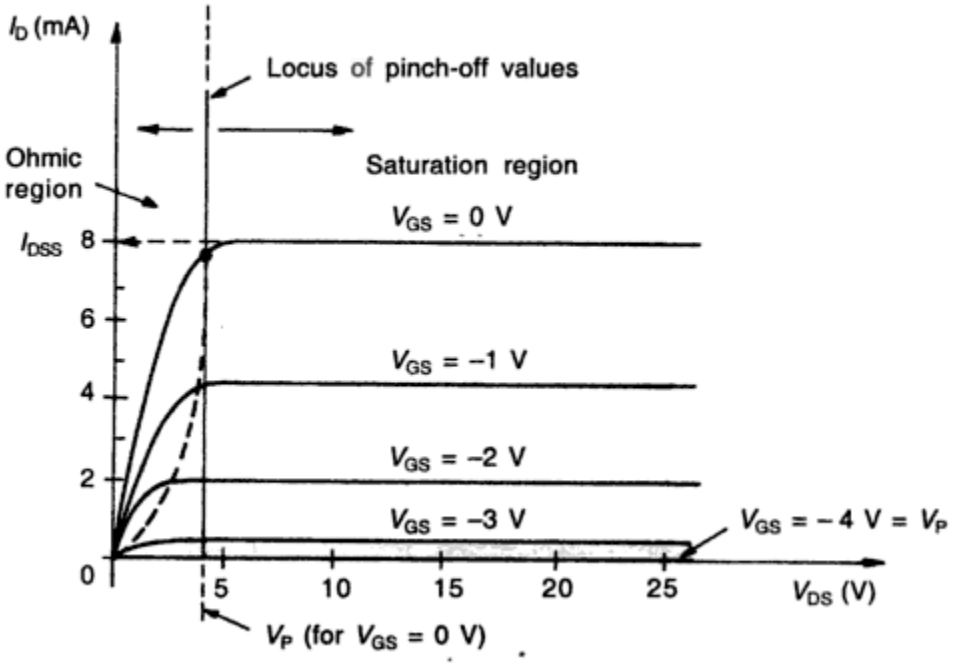
When the gate is shorted to source, there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by I_{DSS} and this is the possible drain current in JFET. It is clear that the gate to source voltage controls the current flowing through the channel and hence FET is also called **voltage controlled current source.**

Characteristics

Drain (or) current voltage characteristics of JFET

The current voltage characteristics of an n-channel JFET is shown in the figure. The drain current (I_D) is plotted with V_{DS} for different values of V_{GS}. This characteristic is also known as drain characteristics of JFET. From the fig, we see that as the voltage increased from 0 to a few volts, the current increases as determined by ohm's law. The

straight nature of the curve at low values for V_{DS} reveals that for this region the resistance is essentially constant for a fixed valued of V_{GS}. But the slope of the I_D - V_{DS} curve near the origin is a function of the gate voltage. This region of operation is known as the linear region or ohmic region. As V_{DS} increases and approaches a value V_P (referred to as pinch – off voltage), slope of the curve changes and the channel resistance increases. If V_{DS} increases beyond pinch-off value, characteristics curve becomes more horizontal and I_D maintains a saturation level. For V_{GS} = 0v , the saturated value of I_D is designated as I_{DSS} , which is the drain – to – source current with source – gate short circuit. Thus, I_{DSS} is the maximum drain current for a JFET, obtained under the conditions V_{GS} = 0V and $V_{DS} > |V_P|$. As the V_{DS} increases beyond V_P, the level of I_D remains essentially the same and this region of the characteristics is known as saturation region. It may also be noted that once $V_{DS} > V_{p,}$ the JFET has the characteristics of a current source. Thus the current – voltage characteristics displayed in fig can be divided into ohmic (linear) and saturation regions with the pinch-off condition as the boundary.



As the negative bias of V_{GS} increases, depletion region forms similar to those to those with V_{GS} = 0 V but at a lower level of $V_{DS.}$ Thus, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}, as shown in the

fig. it is seen that $V_{GS} = -V_P$, the saturation level of I_D is essentially 0mA and the devices have been turned off. The region of the right of the pinch-off locus in figure is normally employed in linear amplifiers. The region to the left of the pinch-off locus is referred to as *voltage controlled resistance region*, where the JFET can be used as voltage-controlled resistor. The channel resistance (R_D) increases with increase of V_{GS} values and empirical relation between the two is given by

$$R_D = \frac{R_0}{[1 - (V_{GS}/V_P)]^2}$$

Where R_0 is the resistance with $V_{GS} = 0$. For an n-channel JFET with $R_0 = 10k\Omega$ at $V_{GS} = -2V$.

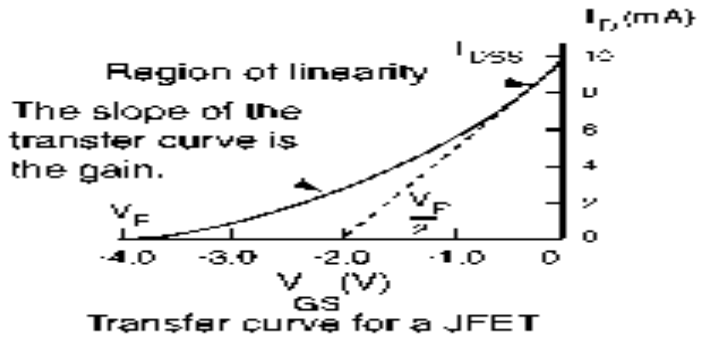
The drain currents suddenly rise in an unbounded manner at very high levels of V_{DS}. The vertical rise in current is an indication that breakdown has occurred and the current through the channel is now limited solely by external circuit. In practical applications, the level of V_{DS} is kept less than the breakdown voltages (V_{DSmax}) that are mentioned in specification sheets of JFET.

Transfer characteristics

The transfer characteristics of JFET is a plot of output (drain) current versus input controlling quantity (gate-source voltage) and is used extensively in JFET amplifiers. In contrast to linear input-output relationship of BJT ($I_C = \beta I_B$), the input-output relationship of JFET is not linear. The relationship between I_D and V_{GS} is defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term on the right-hand side of the equation suggests that the relationship of I_D vs V_{GS} is nonlinear and exponential in nature. The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed. The transfer curve can be obtained using Shockley's equation or from the o/p characteristics.



Transfer curve for a JFET

Expression for pinch off voltage and Drain Current

For the transfer characteristics,V_{DS} is maintained constant at a suitable value greater than the pinch off voltage V_P.The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero. The transfer characteristics I_D versus V_{GS} are shown in figure.

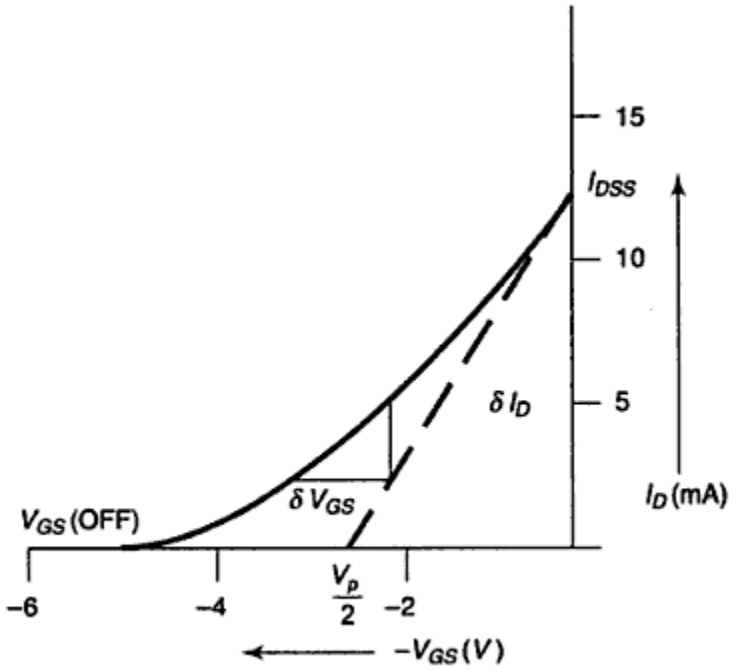


Fig. 7.5 Transfer characteristics of JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (1)$$

Where I_{DS} is the saturation drain current, I_{DSS} is the value of I_{DS} when V_{GS}=0 and V_P is the pinch off voltage

Differentiating eqn (1) with respect to VGS we obtain the expression of gm

$$g_m = -2\, I_{DSS}/V_P(1- V_{GS}/V_P) \quad (2)$$

From eqn (1)

$$(1-V_{GS}/VP)= (I_{DS}/I_{DSS})^{1/2} \quad (3)$$

Suppose $g_m=g_{m0}$ when $v_{GS}=0$

$$g_{mo}=-2I_{DSS}/V_P \quad (4)$$

Therefore from eqn (2) and (4)

$$\mathbf{g_m=g_{m0}(1-V_{GS}/V_P)}$$

MOSFET

MOSFET stands for metal oxide semiconductor field effect transistor. It is capable of voltage gain and signal power gain. The MOSFET is the core of integrated circuit designed as thousands of these can be fabricated in a single chip because of its very small size. Every modern electronic system consists of VLST technology and without MOSFET, large scale integration is impossible.

It is a four terminals device. The drain and source terminals are connected to the heavily doped regions. The gate terminal is connected top on the oxide layer and the substrate or body terminal is connected to the intrinsic semiconductor.

MOSFET has four terminals which is already stated above, they are gate, source drain and substrate or body. MOS capacity present in the device is the main part. The conduction and valance bands are position relative to the Fermi level at the surface is a function of MOS capacitor voltage. The metal of the gate terminal and the sc acts the parallel and the oxide layer acts as insulator of the state MOS capacitor. Between the drain and source terminal inversion layer is formed and due to the flow of carriers in it, the current flows in MOSFET the inversion layer is properties are controlled by gate voltage. Thus it is a voltage controlled device.

Two basic types of MOSFET are n channel and p channel MOSFETs. In n channel MOSFET is current is due to the flow of electrons in inversion layer and in p channel current is due to the flow of holes. Another type of characteristics of clarification can be made of those are enhancement type and depletion type MOSFETs. In enhancement mode, these are normally off and turned on by applying gate voltage. The opposite phenomenon happens in depletion type MOSFETs.

Working Principle of MOSFET

The working principle of MOSFET depends up on the MOS capacitor. The MOS capacitor is the main part. The semiconductor surface at below the oxide layer and between the drain and source terminal can be inverted from p-type to n-type by applying a positive or negative gate voltages respectively. When we apply positive gate voltage the holes present beneath the oxide layer experience repulsive force and the holes are pushed downward with the substrate. The depletion region is populated by the bound negative charges, which are associated with the acceptor atoms. The positive voltage also attracts electrons from the n+ source and drain regions in to the channel. The electron reach channel is formed. Now, if a voltage is applied between the source and the drain, current flows freely between the source and drain gate voltage controls the electrons concentration the channel. Instead of positive if apply negative voltage a hole channel will be formed beneath the oxide layer.

Now, the controlling of source to gate voltage is responsible for the conduction of current between source and the drain. If the gate voltage exceeds a given value, called the three voltage only then the conduction begins.

The current equation of MOSFET in triode region is –

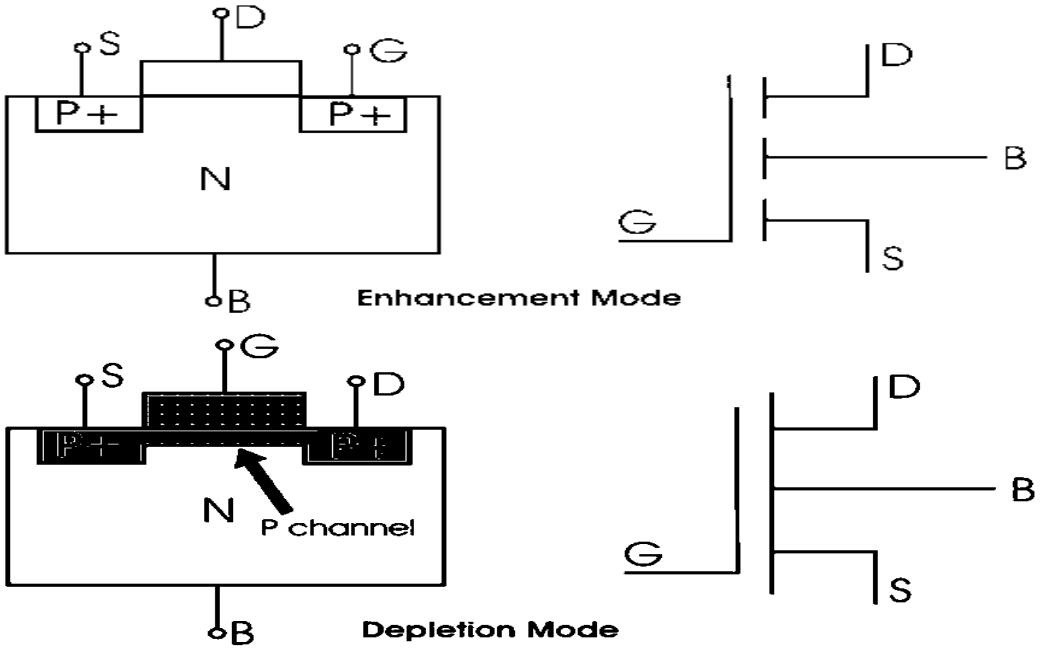
$$I_D = u_n C_{ox} \frac{W}{2}[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]$$

Where, u_n = Mobility of the electrons C_{ox} = Capacitance of the oxide layer W = Width of the gate area L = Length of the channel V_{GS} = Gate to Source voltage V_{TH} = Threshold voltage V_{DS} = Drain to Source voltage.

P-Channel MOSFET

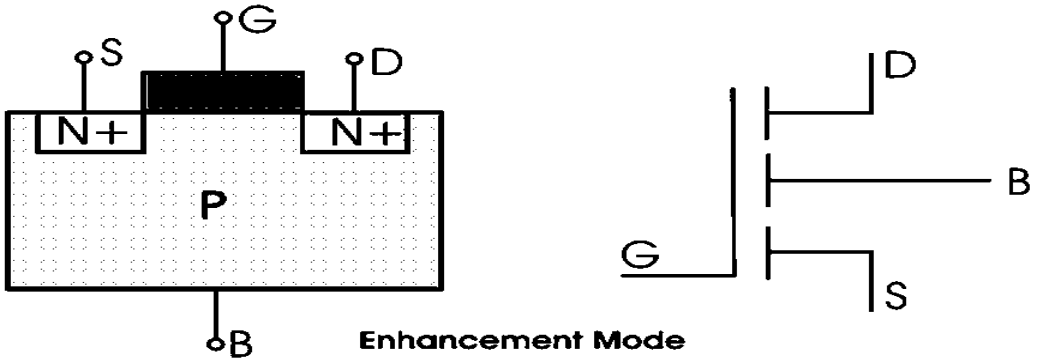
MOSFET which has p - channel region between source any gate is known as **p - channel MOSFET**. It is a four terminal devices, the terminals are gate, drain, source and substrate or body. The drain and source are heavily doped p+ region and the substrate is in n-type. The current flows due to the flow of positively charged holes that's why it is known as p-channel MOSFET. When we apply negative gate voltage, the electrons present beneath the oxide layer, experiences repulsive force and they are pushed downward in to the substrate, the depletion region is populated by the bound positive charges which are associated with the donor atoms. The negative gate voltage

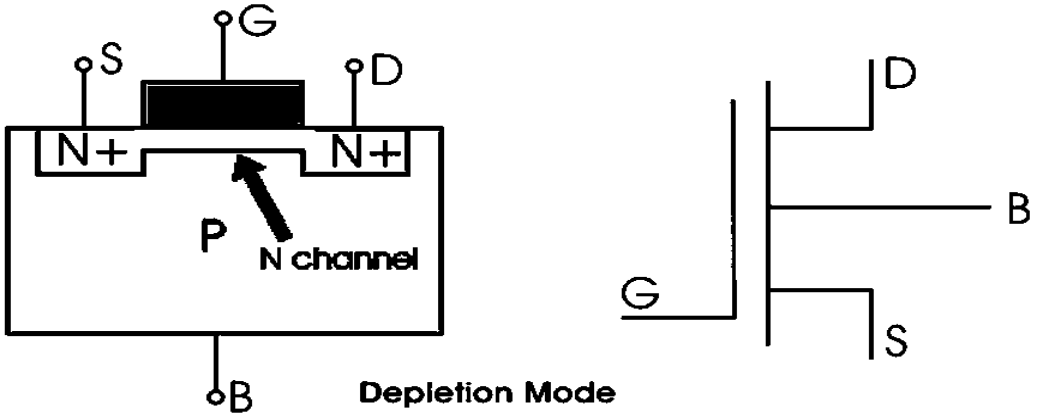
also attracts holes from p+ source and drain region in to the channel region. Thus hole which channel is formed now if a voltage between the source and the drain is applied current flows. The gate voltage controls the hole concentration of the channel. The diagram of p- channel enhancement and depletion MOSFET are given below.



N-Channel MOSFET

MOSFET having n-channel region between source and drain is known as **n-channel MOSFET** . It is a four terminal device, the terminals are gate, drain and source and substrate or body. The drain and source are heavily doped n+ region and the substrate is p-type. The current flows due to flow of the negatively charged electrons, that's why it is known as n- channel MOSFET. When we apply the positive gate voltage the holes present beneath the oxide layer experiences repulsive force and the holes are pushed downwards in to the bound negative charges which are associated with the acceptor atoms. The positive gate voltage also attracts electrons from n+ source and drain region in to the channel thus an electron reach channel is formed, now if a voltage is applied between the source and drain. The gate voltage controls the electron concentration in the channel n-channel MOSFET is preferred over p-channel MOSFET as the mobility of electrons are higher than holes. The diagrams of enhancements mode and depletion mode are given below.

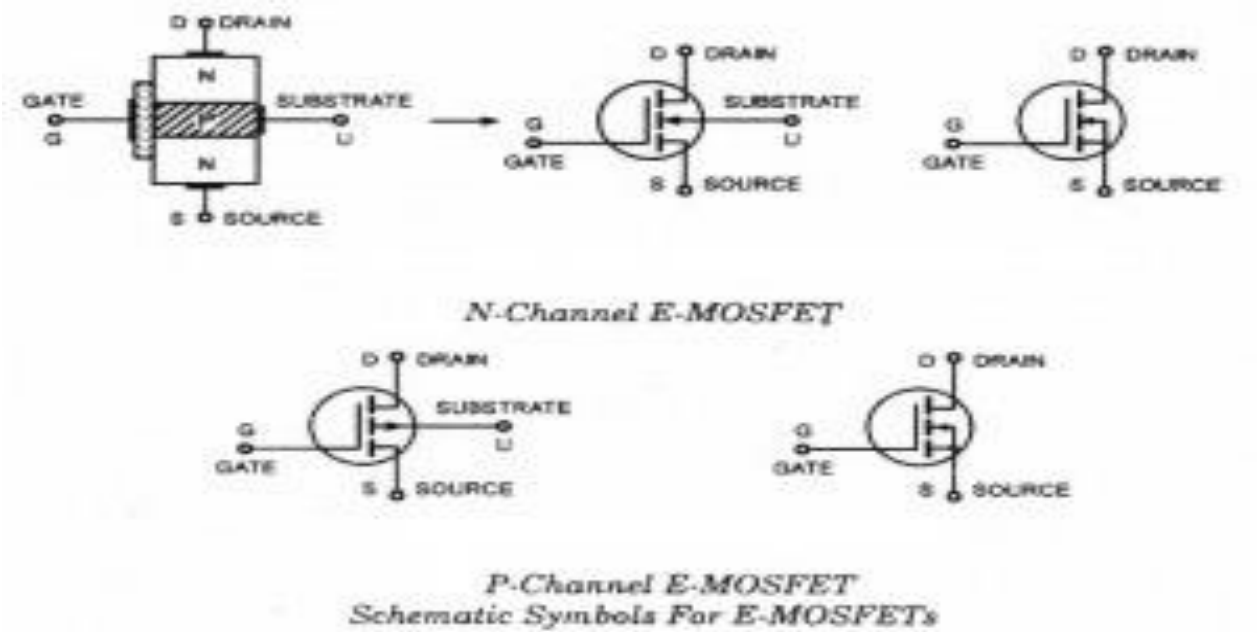




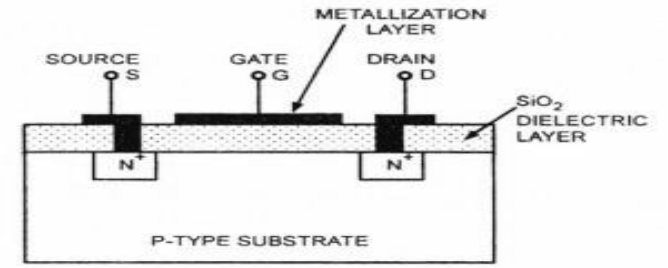
Enhancement and Depletion Mode MOSFET

EMOSFET

Symbol



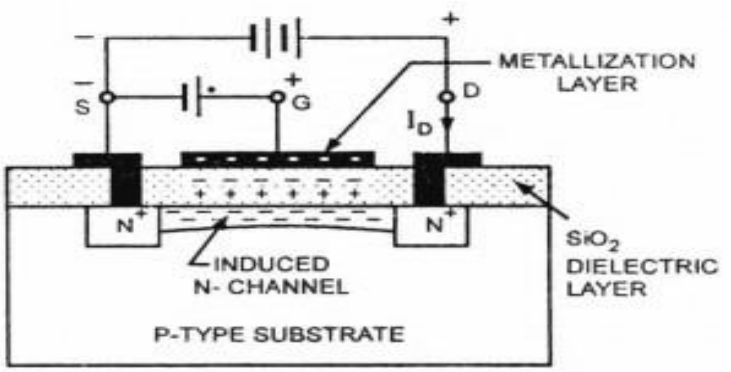
Construction



N-Channel E-MOSFET Structure

Figure shows the construction of an N-channel E-MOSFET. The main difference between the construction of DE-MOSFET and that of E-MOSFET, as we see from the figures given below the E-MOSFET substrate extends all the way to the silicon dioxide (SiO_2) and no channels are doped between the source and the drain. Channels are electrically induced in these MOSFETs, when a positive gate-source voltage V_{GS} is applied to it.

Operation



Operation of N-Channel E-MOSFET

As its name indicates, this MOSFET operates only in the enhancement mode and has no depletion mode. It operates with large positive gate voltage only. It does not conduct when the gate-source voltage $V_{GS} = 0$. This is the reason that it is called normally-off MOSFET. In these MOSFET's drain current I_D flows only when V_{GS} exceeds V_{GST} [gate-to-source threshold voltage].

When drain is applied with positive voltage with respect to source and no potential is applied to the gate two N-regions and one P-substrate from two P-N junctions connected back to back with a resistance of the P-substrate. So a very small drain current that is, reverses leakage current flows. If the P-type substrate is now connected

to the source terminal, there is zero voltage across the source substrate junction, and the¯drain-substrate junction remains reverse biased.

When the gate is made positive with respect to the source and the substrate, negative (i.e. minority) charge carriers within the substrate are attracted to the positive gate and accumulate close to the-surface of the substrate. As the gate voltage is increased, more and more electrons accumulate under the gate. Since these electrons cannot flow across the insulated layer of silicon dioxide to the gate, so they accumulate at the surface of the substrate just below the gate. These accumulated minority charge carriers N -type channel stretching from drain to source. When this occurs, a channel is induced by forming what is termed an inversion layer (N-type). Now a drain current starts flowing. The strength of the drain current depends upon the channel resistance which, in turn, depends upon the number of charge carriers attracted to the positive gate. Thus drain current is controlled by the gate potential.

Since the conductivity of the channel is enhanced by the positive bias on the gate so this device is also called the enhancement MOSFET or E- MOSFET.

The minimum value of gate-to-source voltage V_{GS} that is required to form the inversion layer (N-type) is termed the gate-to-source threshold voltage V_{GST}. For V_{GS} below V_{GST}, the drain current $I_D = 0$. But for V_{GS} exceeding V_{GST} an N-type inversion layer connects the source to drain and the drain current I_D is large. Depending upon the device being used, V_{GST} may vary from less than 1 V to more than 5 V.

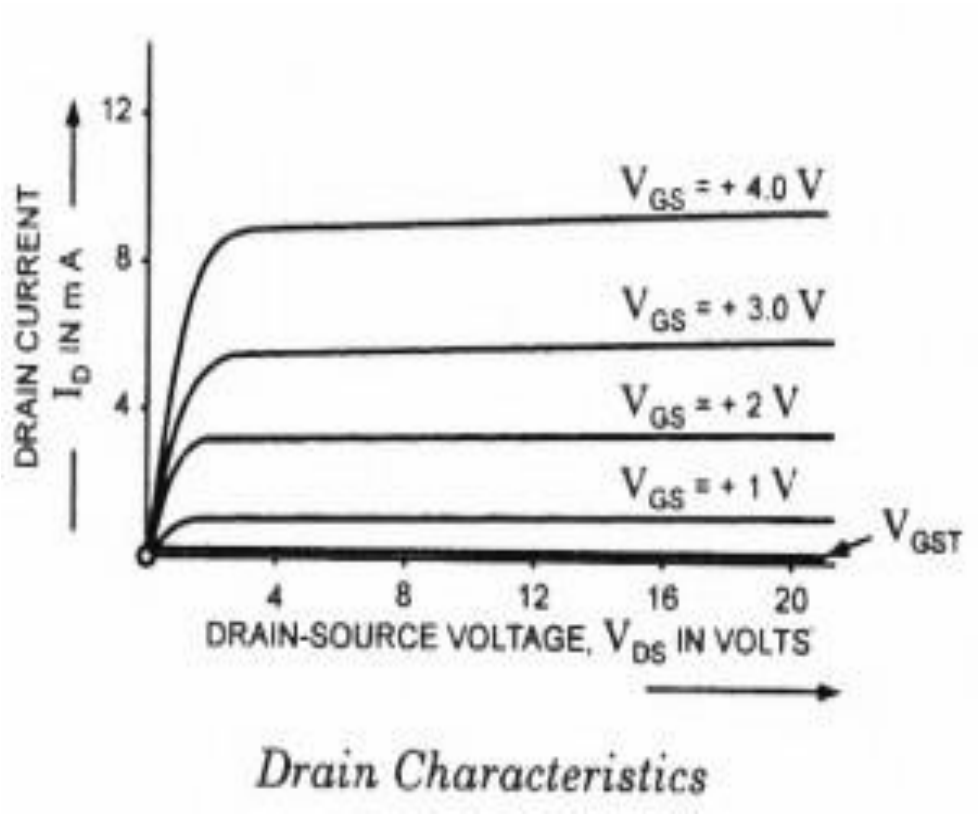
JFETs and DE-MOSFETs are classified as the depletion-mode devices because their conductivity depends on the action of depletion layers. E-MOSFET is classified as an enhancement-mode device because its conductivity depends on the action of the inversion layer. Depletion-mode devices are normally ON when the gate-source voltage $V_{GS} = 0$, whereas the enhancement-mode devices are normally OFF when $V_{GS} = 0$.

Characteristics

Drain Characteristics

Drain characteristics of an N-channel E-MOSFET are shown in figure. The lowest curve is the V_{GST} curve. When V_{GS} is lesser than V_{GST}, I_D is approximately zero. When V_{GS} is greater than V_{GST}, the device turns- on and the drain current I_D is controlled by

the gate voltage. The characteristic curves have almost vertical and almost horizontal parts.



Drain Characteristics

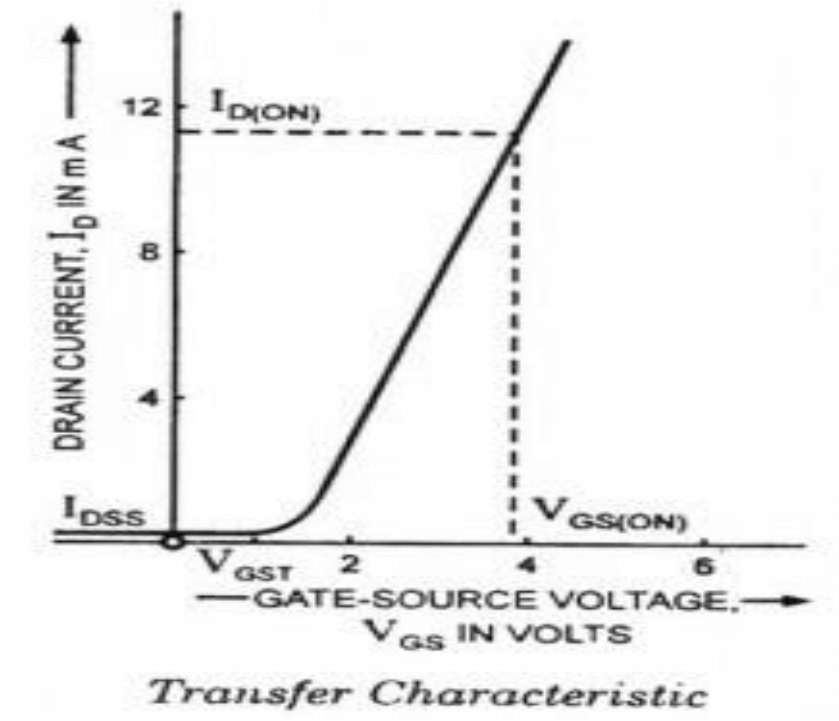
The almost vertical components of the curves correspond to the ohmic region, and the horizontal components correspond to the constant current region. Thus E-MOSFET can be operated in either of these regions *i.e.* it can be used as a variable-voltage resistor (WR) or as a constant current source.

Transfer Characteristics

Figure shows a typical transconductance curve. The current IDSS at VGS <=0 is very small, being of the order of a few nano-amperes. When the V_{GS} is made positive, the drain current I_D increases slowly at first, and then much more rapidly with an increase in V_{GS}. The manufacturer sometimes indicates the *gate-source threshold voltage* V_{GST} at which the drain current I_D attains some defined small value, say 10 u A. A current I_D (0N, corresponding approximately to the maximum value given on the drain characteristics and the values of V_{GS} required to give this current $V_{Gs\ QN}$ are also usually given on the manufacturers data sheet.

The equation for the transfer characteristic does not obey equation. However it does follow a similar “square law type” of relationship. The equation for the transfer characteristic of E-MOSFETs is given as:

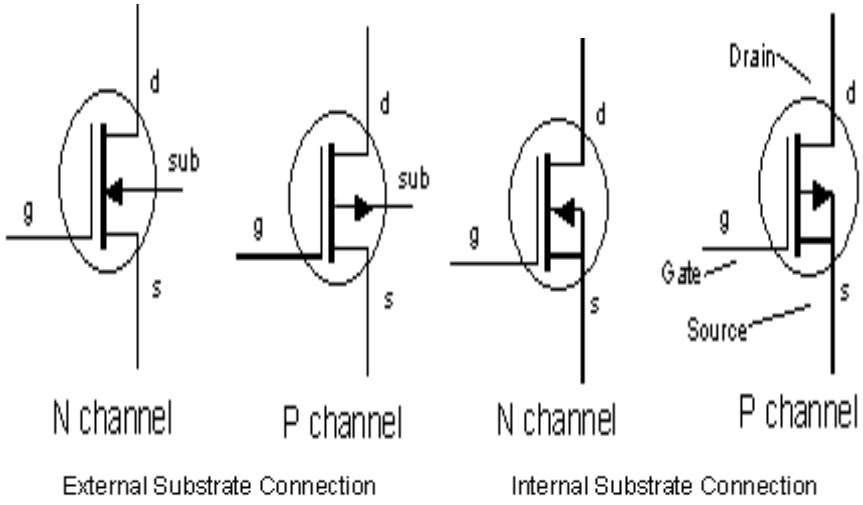
$$I_D=K(V_{GS}-V_{GST})^2$$



Transfer Characteristic

Depletion Mode MOSFET

Symbol



Construction

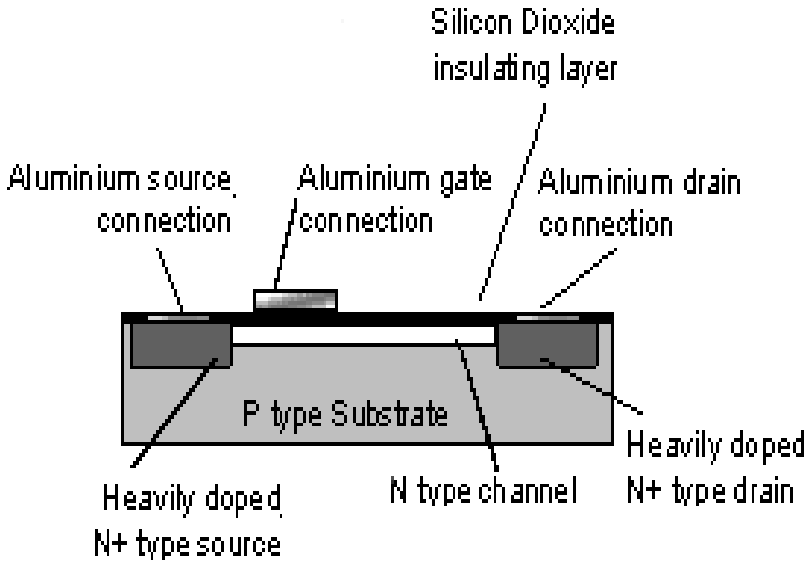


Fig 5.1 Depletion Mode N Channel MOSFET

The depletion mode MOSFET shown as a N channel device (P channel is also available) in Fig 5.1 is more usually made as a discrete component, i.e. a single transistor rather than IC form. In this device a thin layer of N type silicon is deposited just below the gate−insulating layer, and forms a conducting channel between source and drain.

Therefore when the gate source voltage V_{GS} is zero, current (in the form of free electrons) can flow between source and drain. Note that the gate is totally insulated from the channel by the layer of silicon dioxide. Now that a conducting channel is present the gate does not need to cover the full width between source and drain. Because the gate is totally insulated from the rest of the transistor this device, like other IGFETs, has a very high input resistance.

Operation

In the N channel device, shown in Fig. 5.2 the gate is made negative with respect to the source, which has the effect of creating a depletion area, free from charge carriers, beneath the gate. This restricts the depth of the conducting channel, so increasing channel resistance and reducing current flow through the device. Depletion mode MOSFETS are also available in which the gate extends the full width of the channel

(from source to drain). In this case it is also possible to operate the transistor in enhancement mode. This is done by making the gate positive instead of negative.

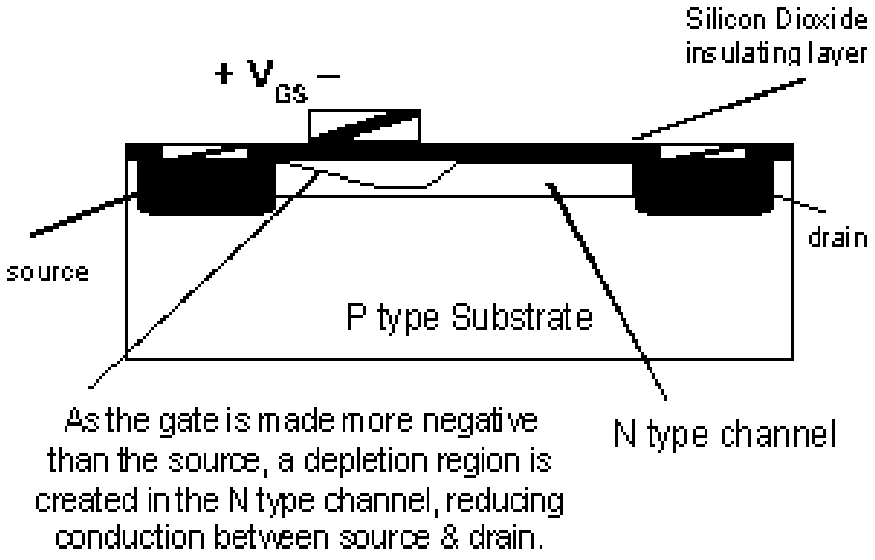
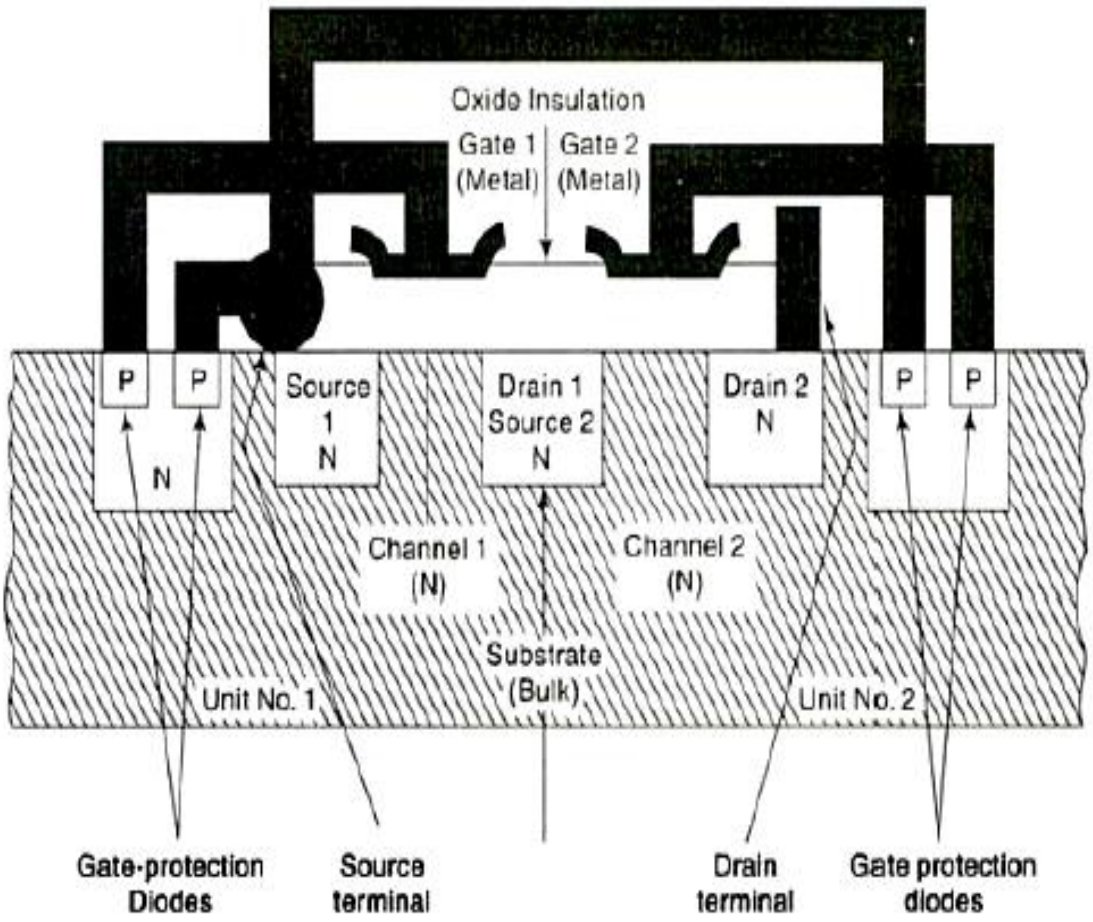


Fig. 5.2 Operation of a Depletion Mode MOSFET

The positive voltage on the gate attracts more free electrons into the conducing channel, while at the same time repelling holes down into the P type substrate. The more positive the gate potential, the deeper, and lower resistance is the channel. Increasing positive bias therefore increases current flow. This useful depletion/enhancement version has the disadvantage that, as the gate area is increased, the gate capacitance is also larger than true depletion types. This can present difficulties at higher frequencies.

Handling Precautions for MOSFET

The MOSFET has the drawback of being very susceptible to overload voltage and may require special handling during installation. The MOSFET gets damaged easily if it is not properly handled. A very thin layer of SiO_2, between the gate and channel is damaged due to high voltage and even by static electricity. The static electricity may result from the sliding of a device in a plastic bag. If a person picks up the transistor by its case and brushes the gate against some grounded objects, a large electrostatic discharge may result.In a relatively dry atmosphere, a static potential of 300V is not uncommon on a person who has high resistance soles on his footwear.



MOSFETs are protected by a shorting ring that is wrapped around all four terminals during shipping and must remain in place until after the devices soldered in position. prior to soldering ,the technician should use a shorting strap to discharge his static electricity and make sure that the tip of the soldering iron is grounded. Once in circuit, there are usually low resistances present to prevent any excessive accumulation of electro static charge .However, the MOSFET should never be inserted into or removed from a circuit with the power ON.JFET is not subject to these restrictions, and even some MOSFETs have a built in gate protection known as “integral gate protection”, a system built into the device to get around the problem of high voltage on the gate causing a puncturing of the oxide layer. The manner in which this is done is shown in the cross sectional view of Fig.7.11.The symbol clearly shows that between

each and the sorce is placed a back-to-back (or front-to-front)pair of diodes, which are built right into P type substrate.

FET as Voltage-Variable Resistor

FET is operated in the constant-current portion of its output characteristics for the linear applications. In the region before pinch-off , where V_{DS} is small , the drain to source resistance rd can be controlled by the bias voltage V_{GS} . The FET is useful as a voltage variable resistor (VVR) or voltage dependent resistor (VDR) .

In JFET , the drain to source conductance $g_d = I_D/V_{DS}$ for small values of V_{DS} , which may also be expressed as

$$g_d = g_{do}[1-(V_{GS}/V_P)^{1/2}]$$

where g_{do} is the value of drain conductance when the bias voltage V_{GS} is zero. The variation of the r_d with V_{GS} can be closely approximated by the empirical expression ,

$$r_d = r_o/(1-KV_{GS})$$

Where r_o=drain resistance at zero gate bias, and K=a constant , dependent upon FET type .

Comparison of MOSFET and JFET

1. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel. In the JFET the transverse electric field across the reverse biased PN junction controls the conductivity of the channel.
2. The gate leakage current in a MOSFET is of the order of 10^{-12}A.Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} ohm. The gate leakage current of a JFET is of the order of 10^{-9}A and its input resistance is of the order of 10^8 ohm.
3. The output characteristics of the JFET are flatter than those of the MOSFET and hence, the drain resistance of a JFET(0.1 to 1Mohm) is much higher than that of a MOSFET(1 to 50 K ohm)
4. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.
5. Comparing to JFET, MOSFETs are easier to fabricate.

6. MOSFET is very susceptible to overload voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.
7. MOSFET has zero offset voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.
8. Special digital CMOS circuits are available which involves near –zero power dissipation and very low voltage and current requirements. This makes them most suitable for portable systems.

Comparison of JFET And BJT

1. FET operations depend only on the flow of majority carrier-holes for P-channel FETs and electrons for N-channel FETs. Therefore, they are called Unipolar devices. Bipolar transistor (BJT) operation depends on both minority and majority current carrier.
2. As FET has no junctions and the conduction is through an N-type or P-type semiconductor material, FET is less noisy than BJT.
3. As the input circuit of FET is reverse biased, FET exhibits as much higher input impedance (in the order of 100MOHM) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can act as excellent buffer amplifier but the BJT has low input impedance because its input circuit is forward biased.
4. FET is a voltage control device, i.e. voltage at the input terminal controls the output current, whereas BJT is a current control device, i.e. the input current controls the output current.
5. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
6. The performance of BJT is degraded by neutron radiations because of reduction in minority carrier life time, whereas FET can tolerate a much higher level of radiation since they do not rely on minority carrier for their operation.
7. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it

prevents the FET from thermal break down. The BJT has a positive temperature coefficient at high current levels which leads to thermal break down.

8. Since FET does not suffer from minority carrier storage effects, it has a higher switching speeds and cut off frequencies.BJT suffers a minority carrier storage effects and therefore has lower switching speed and cut off frequencies.
9. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
10. BJT are cheaper to produce than FETs.