# UNIT 1
## SYLLABUS

**UNIT 1 INTRODUCTION TO OP- AMP AND ITS APPLICATIONS 9 Hrs.**

OP-AMP- DC and AC Characteristics- Input offset voltage- Input bias current-Input offset current- Total output offset voltage- Thermal drift- Slew rate- CMRR -Inverting amplifier- Non-inverting amplifier- Voltage follower- Summing and differential amplifier- Integrator- Differentiator- Logarithmic and Anti logarithmic amplifiers-Comparator and Schmitt trigger.

## TABLE OF TOPICS

## 1.1 INTRODUCTION TO OPERATIONAL AMPLIFIER

### 1.1.1 Integrated Circuit

An Integrated circuit is a miniature electronic circuit comprising of active and passive components irreparably (impossible to rectify or repair) joined together on a single chip of Silicon.

Possible question: *Define Integrated Circuit.*

### 1.1.2 Advantages of Integrated circuits over discrete component circuits

The integrated circuits are advantageous than that of discrete component circuit with some advantages listed below.

1. Miniaturization and hence density of equipment increased. (Since they are of small size, equipment can hold more components within a same area)
2. Cost is reduced when manufactured in batch processing.
3. Improvised system reliability due to elimination of soldered joints.
4. Complex circuits can be fabricated with better characteristics and thus functional performance is improvised.
5. Increased operating speeds due to minimized parasitic capacitance
6. Power consumption minimized.

Possible question: *List the advantages of IC over discrete circuits.*

### 1.1.3 Building Blocks of an Operational Amplifier

An operational amplifier is internally built by four blocks namely

1. Unbalanced differential amplifier,

2. Balanced differential amplifier,

3. Buffer and level translator and

4. Output stage (Push-pull Amplifier) as shown in the figure, fig. 1.4.

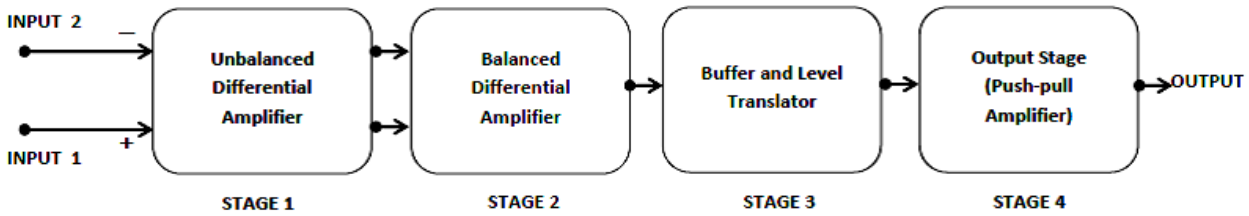


**Fig.1.1.3.** Building blocks of an OP AMP

*Stage 1*

This stage offers high impedance to the input terminals. Since it is an unbalanced amplifier, it amplifies the inputs individually with high impedance and the output shall be fed into next stage of balanced amplifier. (Reference figure, fig.1.1.3.1)

*Stage 2*

Since it is a balanced amplifier, it gives differential output with high gain. This is the stage where high gain is provided and the output is difference between the input signals with low common mode signal. (Reference figure, fig.1.1.3.2)

The above differential amplifiers provide high gain and input impedance with less input current entering into it.

*Stage 3*

This stage comprises of buffer and level shifter circuits.

Level shifter circuit shifts the reference level of a signal. As shown in figure, fig.1.1.3.3, the input reference level 0.0 is shifted to 2.5 in output signal. Thus this circuit can shift the reference level of the input.

Buffer circuit matches an input circuit of impedance low (or high) with an output load of high (or low) impedance. If they both are connected without this buffer matching circuit, the load drains more current from the input circuit leading to shift of operating point which in turn induces unwanted effect.

*Stage 4*

Stage four (output stage) is for improvising current, thus a push-pull complementary symmetry amplifier as shown in figure, fig.1.1.3.4. The amplifier separately amplifies positive and negative cycle with NPN and PNP resistors respectively. During positive cycle, current flows into load resistance $R_L$, but in negative cycle current flows from $R_L$ in opposite direction. Thus by carefully choosing the value of load resistance, $R_L$, the output amplitude can be varied.

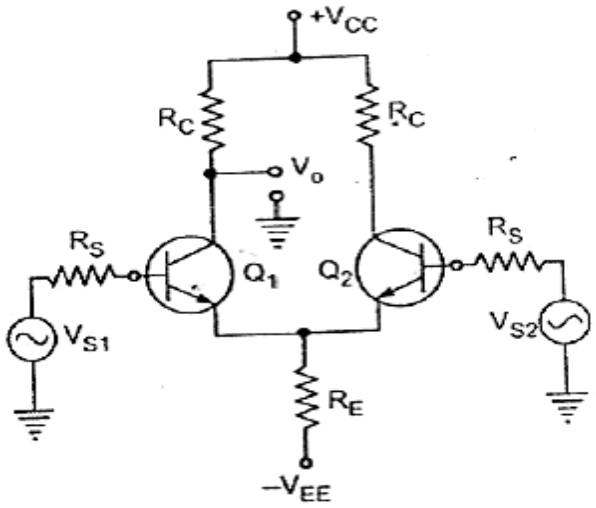


**Fig.1.1.3.1.** Unbalanced Differential Amplifier

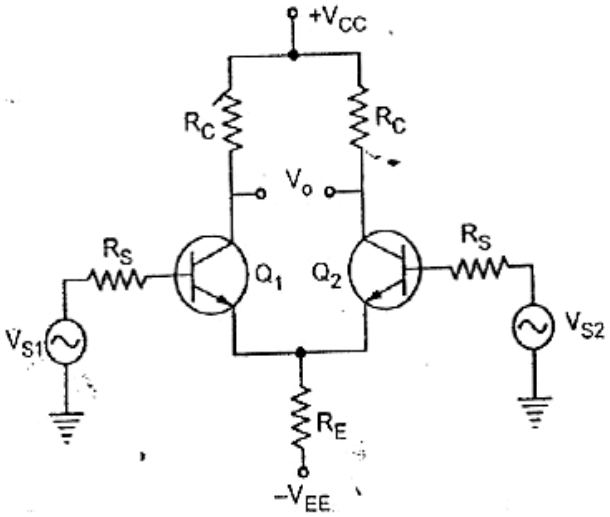


**Fig.1.1.3.2.** Unbalanced Differential Amplifier

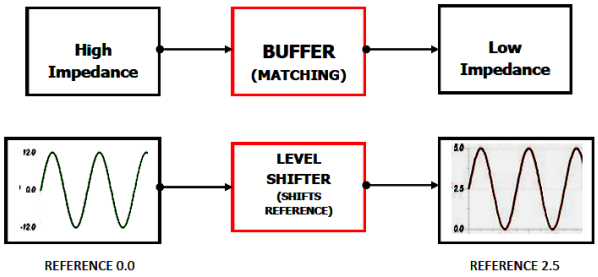


**Fig.1.1.3.3.** Buffer and Level translator

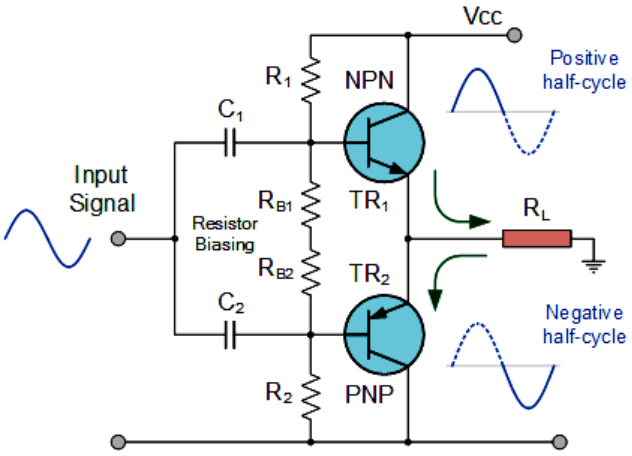


**Fig.1.1.3.4.** Push-pull Amplifier

Possible question: *Elaborately explain the building blocks of an operational amplifier with neat sketches.*

### 1.1.4 Ideal operational amplifier

An Ideal operational amplifier is shown in the figure, fig. 1.1.4.a.

In an ideal op amp,

1. The currents entering the input terminals 1 and 2, $i_1$ and $i_2$ respectively, shall be zero. $i_1=i_2=0$.
2. The voltages between reference and the input terminals 1 and 2, $V_1$ and $V_2$ respectively, shall be equal. $V_1=V_2$.
3. The difference between input terminal voltages, $V_d$ shall be zero. $V_d=V_2 - V_1$.

As per the figure shown as equivalent circuit, fig. 1.1.4.b, input resistance $R_i$, output resistance $R_o$ and open loop gain $A_{OL}$ shall be explained further.

4. Input resistance $R_i$ shall be very high (Ideally $R_i=\infty$)
5. Output resistance $R_o$ shall be very low (Ideally $R_o=0$)
6. Open loop gain $A_{OL}$ shall be very high (Ideally $A_{OL}=\infty$)

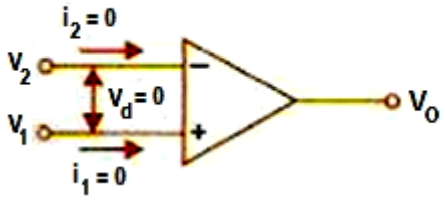


**Fig.1.1.4.a.** Ideal OP AMP

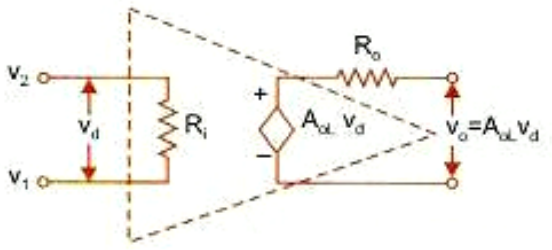


**Fig. 1.1.4.b.** OP AMP equivalent circuit

Thus ideal op amp shall be an infinite gain amplifier with zero input currents, infinite input resistance and zero output resistance.

Possible question: *What are all the characteristics of Ideal operational amplifier?*

## 1.2 DC AND AC CHARACTERISITCS

The two main categories of op amp characteristics are DC and AC Characterisitics.

### 1.2.1 DC Characteristics

DC characteristics are analyzed when input of the op amp is dc signal. The dc characteristics of op amp and thus it shall be discussed in following section.

#### *1.2.1.1 Input offset voltage ($V_{IOS}$)*

The dc voltage connected any one of the input terminal to make the output offset voltage.

When output offset voltage is more than zero, the non-inverting terminal is supposed to have higher potential than that of inverting terminal due to internal imbalance. So input offset voltage is connected to inverting terminal to compensate the offset and the output voltage to zero.

When output offset voltage is less than zero, the inverting terminal is supposed to have higher potential than that of non-inverting terminal due to internal imbalance. So input offset voltage is connected to non-inverting terminal to compensate the offset and the output voltage to zero.

Thus this dc input offset voltage is known as compensating voltage for output offset voltage.

Possible question: *Define Input offset voltage, input offset current, input bias current and output offset voltage.*

#### *1.2.1.2 Input bias current ($I_B$)*

For an ideal op amp, the dc currents entering the input terminals shall be zero. But practically a minimum amount of current enters the terminals and they are termed as bias currents.

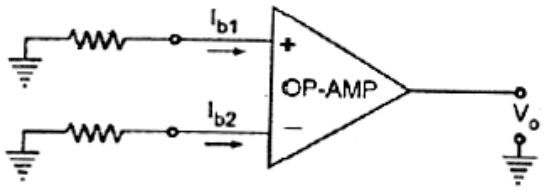


**Fig. 1.2.1.2.a.** Input bias currents

The bias current entering non-inverting terminal is $I_{b1}$ and entering inverting terminal is $I_{b2}$. These currents flow into the respective terminals when both input terminals are grounded. The total input bias current is the average currents entering into both the terminals.

$$I_B = \frac{|I_{b1}|+|I_{b2}|}{2} \qquad \text{(Eq.1.2.1.2)}$$

#### *1.2.1.3 Input offset current ($I_{IOS}$)*

Input dc offset current is the difference between the magnitudes of bias currents $I_{b1}$ and $I_{b2}$ as shown in the equation 1.2.1.3. Practically this current is very small in magnitude in the order of nano-amperes.

$$I_b = |I_{b1} - I_{b2}| \qquad \text{(Eq.1.2.1.3)}$$

#### *1.2.1.4 Total Output offset voltage ($V_{OOS}$)*

As shown in the figure, fig.1.2.1.2.a, when both the inputs are connected to ground potential, the output dc voltage $V_o$ should be zero ideally. But practically the output voltage is not zero. The value of this output voltage is termed as Total output offset voltage.

### 1.2.2 AC characteristics

AC characteristics are analyzed when input of the op amp is ac signal. Slew rate is a major ac characteristic of op amp and thus it shall be discussed in next section.

#### 1.2.2.1 Slew rate

Slew rate is defined as the maximum rate of change of output voltage with time.

For this, a voltage follower circuit is chosen where output is fed-back directly to inverting terminal and the inverting terminal is connected to a rectangular pulse of 50% duty cycle (Square wave) as shown in figure, fig.1.2.2.1.a.

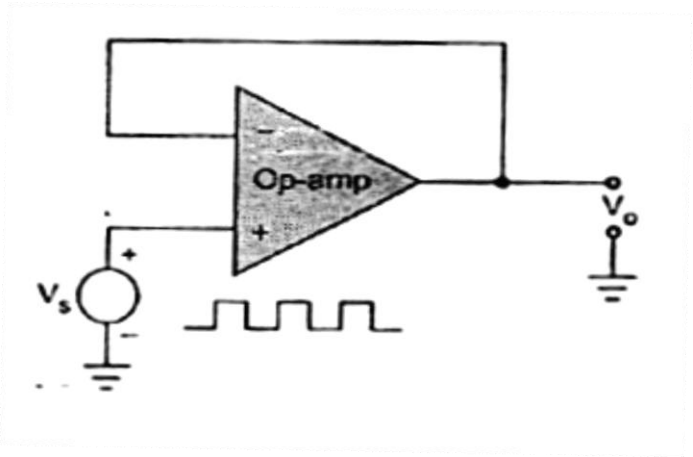


**Fig. 1.2.2.1.a Measurement of slew rate of OP AMP**

The output $V_o$ is to follow the input. But as shown in figure, fig.1.2.2.1.b, the output wave is distorted and not a rectangular wave as input. Thus the variation of output is denoted by $dV_o$, change in voltage with change in time dt. Thus maximum change in output voltage with change in time is

$$\text{Slew rate} = S = \left.\frac{dV_o}{dt}\right|_{max}$$

This is due to charging and discharging rate of an internal capacitance C of the op amp. The capacitor charges to maximum current $I_{max}$ due to the input voltage fed in the capacitor. The sudden change in input voltage from low to high, allows the capacitor to charge to its maximum. Thus change in output voltage $dV_o/dt$ mainly depends upon charging current $I_{max}$ and the capacitance C.

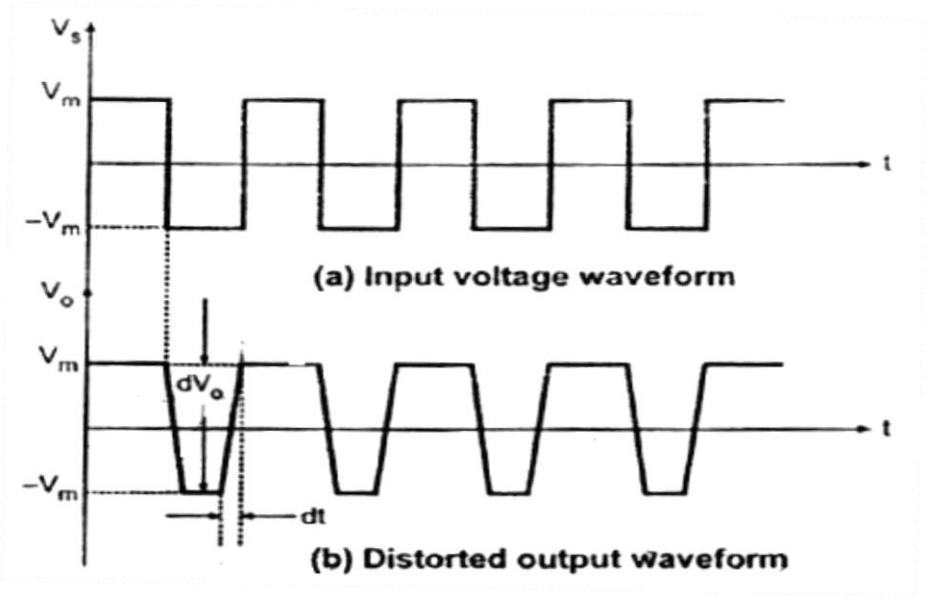


**Fig. 1.2.2.1.b.** slew rate waveforms

Thus slew rate in terms of internal capacitance C is

$$S = \frac{I_{max}}{C}$$

## Slew Rate Equation

Let the input voltage $V_s$ is purely sinusoidal. In this case the output voltage $V_o$ will be also purely sinusoidal, as the circuit used to derive the equation is **voltage follower** circuit as shown in the fig.1.2.2.1 (a). in such circuit output voltage follows input voltage.

So

$$V_s = V_m sin\omega t$$

And

$$V_o = V_m sin\omega t$$

$$\frac{dV_o}{dt} = V_m(\omega cos\omega t)$$

But $\left[\frac{dV_o}{dt}\right]$ maximum is nothing but the slew rate S. **For maximum** $\left[\frac{dV_o}{dt}\right]$, in the equation above cos(ωt) must be maximum. i.e.1.

$$S = \left[\frac{dV_o}{dt}\right]_{max} = \omega V_m$$

$$\boxed{S = 2\pi f V_m \ \ V/sec}$$

This is required **slew-rate equation.**

For the distortion free output, the maximum allowable frequency of operation $f_m$ can be decided by the slew rate.

**Methods of improving Slew rate**

It is known that the slew rate is given by,

$$S = \frac{I_{max}}{C}$$

For understanding the methods of improving slew rate consider the op-amp model for the analysis of the slew rate as shown in the Fig. 1.2.2.3.

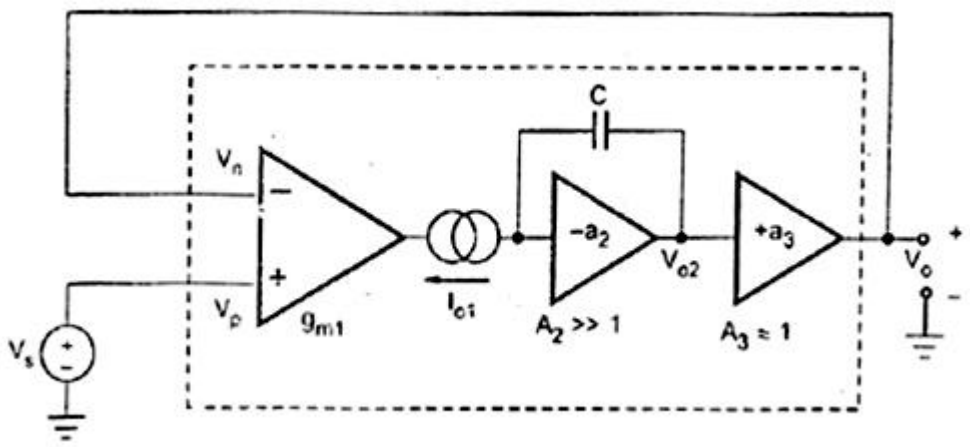


**Fig.1.2.2.3 Op-amp model for slew rate analysis**

The op-amp used is in voltage follower mode in which the output $V_o = V_i$. The circuit is similar to that used earlier to derive slew rate equation, only the op-amp is replaced by its model.

When input overdrives the input stage then $I_{max} = \pm I_{01}$ **(sat)** which are saturation current levels of the input stage. Under this condition, op-amp is said to be operating under large-signal conditions.

The saturation of the input stage limits the slew rate because under saturation condition, the rate at which capacitor C can charge or discharge, according to the input overdrive is at its maximum.

From the fig.1.2.2.3, we can write,

$$I_{01}(sat) = C\frac{dV_{02}}{dt}$$

$$\therefore \frac{dV_{02}}{dt} = \frac{I_{01}(sat)}{C}$$

This rate of change of $V_{02}$ is maximum, due to the saturation effect.

Now the gain of the third stage $a_3 \approx 1$, hence $V_0 = V_{02}$,

$$\therefore \left.\frac{dV_{02}}{dt}\right|_{max} = \frac{dV_{02}}{dt} = \frac{I_{01}(sat)}{C}$$

But maximum rate of change of output voltage is the slew rate.

$$S = \frac{I_{01}(sat)}{C}$$

Analyzing the op-amp model used, we can write,

$$V_{02} = drop\ across\ C = I_{01}Z_C$$

The input stage is a **transconductance amplifier**. i.e. voltage input, current output amplifier. For sufficiently small differential input voltage the relation between input voltage and output current for such an amplifier is,

$$Output\ Current = g_m(differential\ Input)$$

For input stage

$$\therefore I_{01} = g_{m1}(V_p - V_n)$$

$$\therefore V_{02} = Z_C g_{m1}(V_p - V_n)$$

But

$$V_{02} \approx V_o as\ a_3 \approx 1$$

$$\therefore V_0 = Z_C g_{m1}(V_p - V_n)$$

$$V_0 = \left[\frac{1}{j\omega C}\right] g_{m1}(V_p - V_n)$$

As

$$Z_C = X_C = \left[-\frac{j}{\omega C}\right] = \frac{1}{j\omega C}$$

$$\therefore Op - amp\ gain = \frac{|V_o|}{|V_p - V_n|}$$

$$\therefore |a| = \frac{|V_o|}{|V_p - V_n|} = \frac{g_{m1}}{\omega C} = \frac{g_{m1}}{2\pi f C}$$

$$\therefore |a|f = \frac{g_{m1}}{2\pi C}$$

Now the gain-bandwidth product of op-amp is denoted as $f_t$ given by the product of gain |a|and bandwidth f **as**

$$f_t = |a|f$$

$$\therefore f_t = \frac{g_{m1}}{2\pi C}$$

$$\therefore C = \frac{g_{m1}}{2\pi f_t}$$

The gain-bandwidth product is also called **unity gain-bandwidth of op-amp**.

Substituting value of C in the slew-rate

$$\therefore S = 2\pi \frac{I_{01(sat)}}{g_{m1}} f_t$$

Here in the above equation Saturation current $I_{01(sat)}$, mutual conductance $g_{m1}$, and gain-bandwidth product $f_t$ of the op amp can be set in accordingly to improve *slew rate.*

Improving slew rate by

1. Increasing saturation current $I_{01(sat)}$: This is very tough to increase because this may affect the operating point of the transistors used in the circuit.

2. Increasing gain-bandwidth product $f_t$: This is done by using feed-forward compensation. That is two op amps connected in series that one's output is fed into other. This improves the bandwidth by increasing gain-bandwidth product, thus improving slew rate.

3. Decreasing mutual conductance $g_{m1}$ *:* This is done by replacing BJT by FET's. Normally FET's are having less mutual conductance $g_m$ *by improving slew rate.*

Possible question: *Define slew rate and write the slew rate equation. Explain about the methods of improving slew rate.*

### 1.2.2.2 Thermal drift

In op amp, effect of variation in all parameters is severe due to variations in temperature.

***Effect on input offset voltage***

Input offset voltage varies with variation in temperature and thus ratio of change in input offset voltage to change in temperature is termed as *thermal drift on input offset voltage.*

$$Input\ offset\ voltage\ drift = \frac{\Delta V_{ios}}{\Delta T} \qquad \text{(Eq.1.2.2.2.1)}$$

Where $\Delta T$ - change in temperature, $\Delta V_{ios}$ - change in input offset voltage

***Effect on input offset current***

Input offset current varies with variation in temperature and thus ratio of change in input offset current to change in temperature is termed as *thermal drift on input offset current.*

$$Input\ offset\ current\ drift = \frac{\Delta I_{ios}}{\Delta T} \qquad \text{(Eq.1.2.2.2.2)}$$

Where $\Delta T$ - change in temperature, $\Delta I_{ios}$ - change in input offset current

*Effect on input bias current*

Input bias current varies with variation in temperature and thus ratio of change in input bias current to change in temperature is termed as *thermal drift on input bias current.*

$$Input\ bias\ current\ drift = \frac{\Delta I_{ib}}{\Delta T} \qquad \text{(Eq.1.2.2.2.3)}$$

Where $\Delta T$ - change in temperature, $\Delta I_{ib}$ - change in input bias current

*Effect on slew rate*

Slew rate varies with variation in temperature and thus ratio of change in slew rate to change in temperature is termed as *thermal drift on slew rate.*

$$slew\ rate\ drift = \frac{\Delta S}{\Delta T} \qquad \text{(Eq.1.2.2.2.4)}$$

Where $\Delta T$ - change in temperature, $\Delta S$- change in slew rate

Possible question: *Explain Thermal drift on various parameters of op amp.*

### 1.2.2.3 Common Mode Rejection Ratio -CMRR

When the same voltage is applied to both the terminals of op amp, then the op amp is said to be operated in common mode configuration. Op amp is to be operated only in differential mode and common mode signals shall be noise or disturbance signal. The ability of differential amplifier is to reject the common mode signal and expressed as a ratio termed as Common mode rejection ratio (CMRR).

It is defined as ratio of the differential voltage gain ($A_d$) to common mode voltage gain ($A_c$).

$$CMRR = \rho = \left|\frac{A_d}{A_c}\right| \qquad \text{(Eq.1.2.2.3.1)}$$

$$CMRR\ in\ dB = 20log\left|\frac{A_d}{A_c}\right| in\ dB \qquad \text{(Eq.1.2.2.3.2)}$$

Practically CMRR should be larger and ideally it shall be $\infty$.

Possible questions: *Define CMRR.*

## Open loop and closed loop configurations

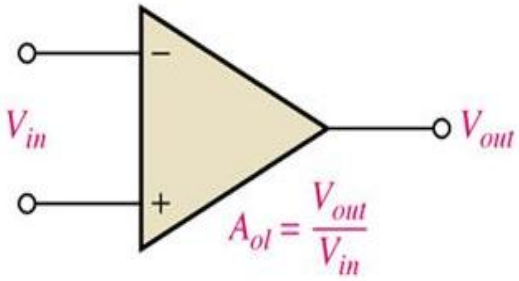


**Fig.1.2.3.a** Open loop configuration

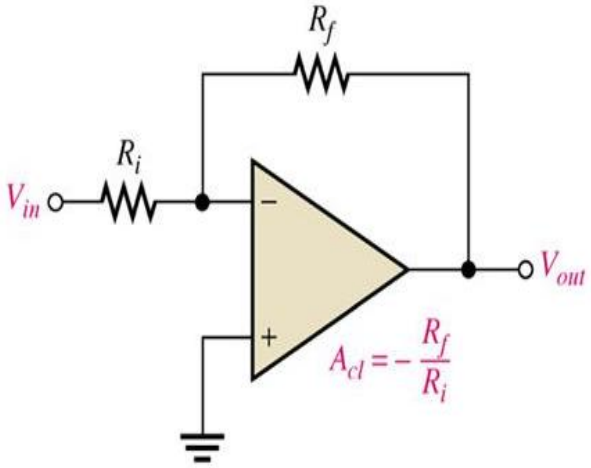


**Fig.1.2.3.b** Closed loop configuration

### Open loop configuration

As shown in figure, fig.1.2.3.a, $V_{in}$ is the input given between input terminals and $V_{out}$ is the output derived. The open loop gain $A_{ol}$ is ratio of the output voltage ($V_{out}$)to the input voltage ($V_{in}$).

$$\text{The open loop gain, } A_{ol} = \frac{V_{out}}{V_{in}} \qquad \text{(Eq.1.2.3.1)}$$

As stated above in eq.1.2.3.1, the gain cannot be controlled or changed. Thus this gain is implicit (in-built) and never be changed explicitly. This gain is very large in terms of 10000.

### Closed loop configuration

As shown in figure, fig.1.2.3.b, $V_{in}$ is the input given into inverting terminal through a resistance $R_i$ and a feed-back resistor $R_f$ connected between output terminal and inverting terminal. $V_{out}$ is the output derived. The open loop gain $A_{cl}$ is ratio of the feed-back resistor ($R_f$) to the resistance ($R_i$). The feedback is *negative*.

$$\text{The closed loop gain, } A_{cl} = -\frac{R_f}{R_i} \qquad \text{(Eq.1.2.3.2)}$$

As stated above in eq.1.2.3.2, the gain now can be controlled or changed. Thus this gain is explicit and by changing the resistor values, gain can be altered.

Thus closed loop gain is advantageous over open loop gain because it can be changed by changing resistor values.

Possible question: *Elaborately explain open loop and closed loop configurations of an op amp with neat sketches.*

## 1.3.1 OP-AMP used in mathematical operations

## 1.3.1 Inverting Amplifier

The amplifier in which the output is inverted i.e. having 180$^o$ phase shift with respect to the input is called an inverting amplifier.

This is possibly the most widely used of all the op-amp circuits. The circuit is shown in Fig. 1.3.1.The output voltage $V_o$ is fed back to the inverting input terminal through the $R_f$ – $R_1$ network where $R_f$ is the feedback resistor. Input signal $v_i$ is applied to the inverting input terminal through $R_1$ and non-inverting input terminal of op-amp is grounded.

Assume an ideal op-amp. As $V_d = 0$, node 'a' is at ground potential and the current $i_1$ through $R_1$ is

$$i_1 = \frac{v_i}{R_1}$$

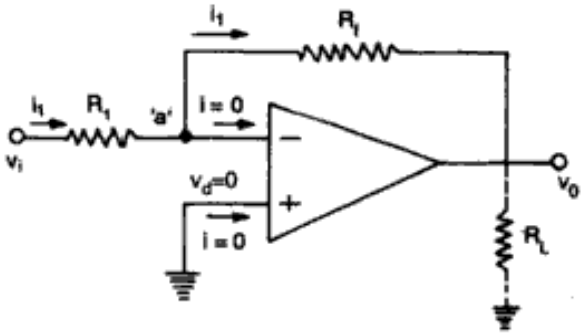


Fig. 1.3.1. Inverting amplifier

Also since op-amp draws no current, all the current flowing through $R_1$ must flow through $R_f$. The output voltage is given by

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1}$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is given by

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

Alternatively, the nodal equation at the node 'a' in Fig. 1.3.1 is given by

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where $v_a$ is the voltage at node 'a'. Since node 'a' is at virtual ground $v_a$=0. Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

### 1.3.2 Non-Inverting Amplifier

The amplifier in which the output is amplified without any phase shift in between input and output is called non inverting amplifier.

If the signal is applied to the non-inverting input terminal and feedback is given as shown in Fig. 1.3.2. The circuit which amplifies without inverting the input signal. It may be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.

As the differential voltage $V_d$ at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 1.3. 2. is $V_i$ same as the input voltage applied to non-inverting input terminal. Now $R_f$ and $R_1$ form a potential divider. Hence

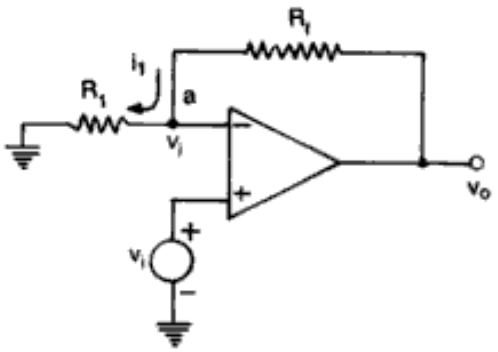


Fig. 1.3.2 Non-inverting amplifier

$$v_i = \frac{v_o}{R_1 + R_f} R_1$$

As no current flows into the op-amp.

$$\frac{v_o}{v_i'} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1}$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1}$$

The gain can be adjusted to unity or more, by proper selection of resistors $R_f$ and $R_1$. Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large ($=\infty$) as the op-amp draws negligible current from the signal source.

### 1.3.3 Voltage Follower

In the non-inverting amplifier of Fig. 1.3.1, if $R_f = 0$ and $R_1 = \infty$, we get the modified circuit of Fig. 1.3.3. The voltage equation becomes

$$v_0 = v_i$$

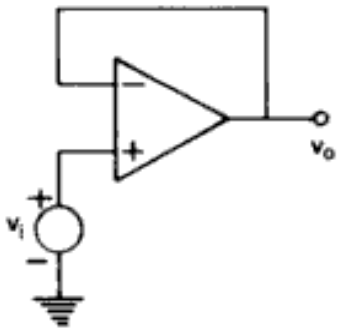


Fig. 1.3.3. Voltage follower

That is, the output voltage is equal to input voltage, both in magnitude and phase. In other words, we can also say that the output voltage follows the input voltage exactly. Hence, the circuit is called a voltage follower. The use of the unity gain circuit lies in the fact that its input impedance is very high (i.e. MΩ order) and output impedance is zero. Therefore, it draws negligible current from the source. Thus a voltage follower may be used as buffer for impedance matching, that is, to connect a high impedance source to a low impedance load.

### 1.3.4 SUMMING AMPLIFIER

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. An inverting summer or a non-inverting summer may be obtained as discussed now.

#### 1.3.4.1 Inverting summing amplifier

A typical summing amplifier with three input voltages $V_1$, $V_2$ and $V_3$, three input resistors $R_1$, R2, R3 and a feedback resistor $R_f$ is shown in Fig. 1.3.4.1. The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$ and $R_i = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor $R_{Comp}$ and hence the non-inverting input terminal is at ground potential.

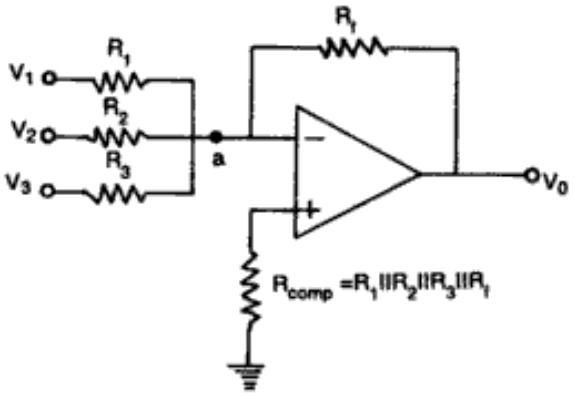


Fig. 1.3.4.1 Inverting Summing Amplifier

The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}+\frac{V_o}{R_f}=0$$

$$V_o=-\left(\frac{R_f}{R_1}V_1+\frac{R_f}{R_2}V_2+\frac{R_f}{R_3}V_3\right)$$

Thus the output is an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$ , we have

$$V_o=-(V_1+V_2+V_3)$$

in which case the output $V_o$. is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f,$$

in which case

$$V_o=-\left(\frac{V_1+V_2+V_3}{3}\right)$$

Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current is compensated by using resistor $R_{comp}$. To find $R_{comp}$, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \text{II} R_2 \text{II} R_3$.Therefore $R_{comp} = R_i \text{II} R_f = R_1 \text{II} R_2 \text{II} R_3 \text{II} R_f$.

**Design an adder circuit using an op-amp to get the output expression as**

$$V_o = -(0.1\ V_1 + V_2 + 10\ V_3)$$

**where $V_1$, $V_2$, and $V_3$ are the inputs.**

**Solution**

**The output in Fig. 4.2 (a) is**

$$V_o = -[(R_f/R_1)\ V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$$

**say** $R_f = 10\ \text{k}\Omega,\ R_1 = 100\ \text{k}\Omega,\ R_2 = 10\ \text{k}\Omega,\ R_3 = 1\ \text{k}\Omega$

**Then the desired output expression is obtained.**

### 1.3.4.2 Non-inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier and is shown in fig.1.3.4.2. Let the voltage at the (-) input terminal be $V_a$. The voltage at (+) input terminal will also be $V_a$. The nodal equation at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

From which we have

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

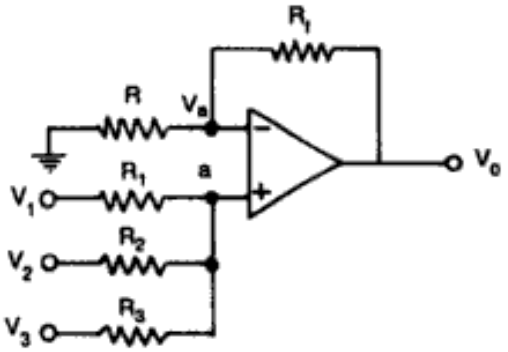


Fig. 1.3.4.2 Non-inverting summing amplifier

The op-amp and two resistors $R_f$ and $R$ constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a$$

Therefore, the output voltage is

$$V_o = \left(1 + \frac{R_f}{R}\right) \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

which is a non-inverted weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f / 2$. Then, $V_o = VI + V2 + V_3$

### 1.3.5 Differential Amplifier (Subtracting Amplifier)

The basic difference amplifier can be used as a subtractor or subtracting amplifier as shown in below fig.1.3.5

If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output $V_{01}$ due to $V_1$ alone, make $V_2$=0. Then the circuit of fig.1.3.5 becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{01} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1$$

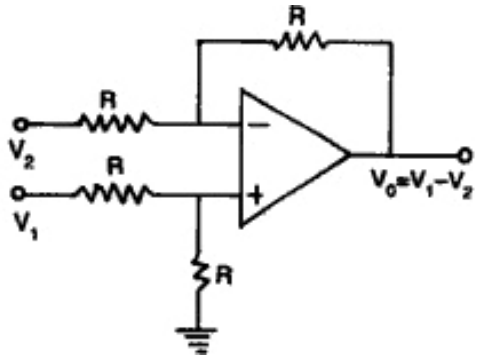


Fig.1.3.5 Subtractor or Subtracting Op-amp

Similarly the output $V_{02}$ due to $V_2$ alone (with $V_1$ grounded) can be written simply for an inverting amplifier as

$$V_{02} = -V_2$$

Thus the output voltage $V_0$ due to both the inputs can be written as

$$V_0 = V_{01} + V_{02} = V_1 - V_2$$

Hence the output voltage $V_o$ is subtraction of input voltages $V_1$ and $V_2$.

## 1.3.6 DIFFERENTIATOR

One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform. A differentiator circuit is shown in Fig. 1.3.6.

The node $N$ is at virtual ground potential i.e., $v_N = 0$. The current $i_C$ through the capacitor is,

$$i_C = C_1 \frac{d}{dt}(v_i - v_N) = C_1 \frac{dv_i}{dt}$$

The current $i_f$ through the feedback resistor is $v_o/R_f$ and there is no current into the op-amp. Therefore, the nodal equation at node $N$ is,

$$C_1 \frac{dv_i}{dt} + \frac{v_o}{R_f} = 0$$

from which we have

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

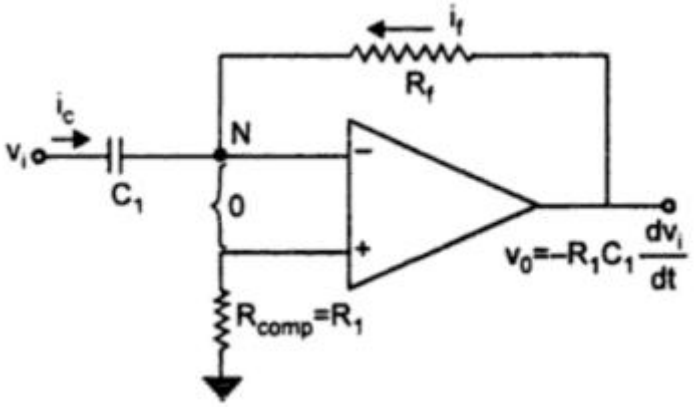


Fig. 1.3.6 Differentiator

Thus the output voltage $v_o$ is a constant $(-R_f C_1)$ times the derivative of the input voltage $v_i$ and the circuit is a differentiator. The minus sign indicates a 180° phase shift of the output waveform $v_o$ with respect to the input signal.

The phasor equivalent is, $V_o(s) = -R_f C_1 s V_i(s)$ where $V_o$ and $V_i$ is the phasor representation of $v_o$ and $v_i$. In steady state, put $s = j\omega$. We may now write the magnitude of gain $A$ of the differentiator as,

$$|A| = \left|\frac{V_o}{V_i}\right| = \left|-j\omega R_f C_1\right| = \omega R_f C_1$$

one can draw the frequency response of the op-amp differentiator. Equation (4.70) may be rewritten as

$$|A| = \frac{f}{f_a}$$

where $$f_a = \frac{1}{2\pi R_f C_1}$$

At $f = f_a$, $|A| = 1$, i.e., 0 dB, and the gain increases at a rate of +20 dB/decade. Thus at high frequency, a differentiator may become unstable and break into oscillation. There is one more problem in the differentiator of Fig. The input impedance (i.e., $1/\omega C_1$) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

### 1.3.6.1 Practical Differentiator

A practical differentiator of the type shown in Fig. eliminates the problem of stability and high frequency noise.

The transfer function for the circuit in Fig. is given by,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{Z_i} = -\frac{s R_f C_1}{(1 + s R_f C_f)(1 + s C_1 R_1)}$$

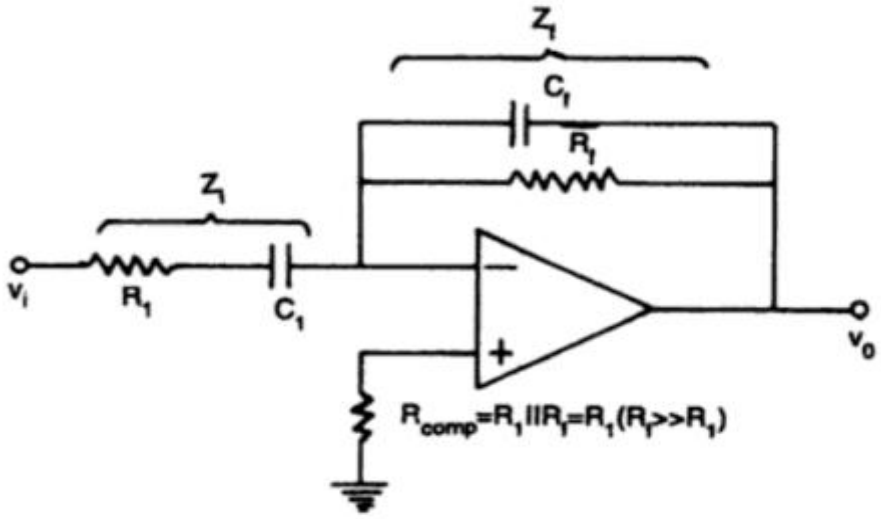


Fig. 1.3.6.1 Practical Differentiator

For $R_f C_f = R_1 C_1$, we get

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_fC_1}{(1+sR_1C_1)^2} = -\frac{sR_fC_1}{\left(1+j\frac{f}{f_b}\right)^2}$$

where, $$f_b = \frac{1}{2\pi R_1 C_1}$$

From Eq. it is evident that the gain increases at +20 dB/ decade for frequency $f < f_b$ and decreases at –20 dB/decade for $f > f_b$ as shown by dashed lines in Fig. . This 40 dB/decade change in gain is caused by $R_1 C_1$ and $R_f C_f$ factors. For the basic differentiator of Fig. the frequency response would have increased continuously at the rate of +20 dB/decade even beyond $f_b$ causing stability problem at high frequency. Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems. The value of $f_b$ should be selected such that,

$$f_a < f_b < f_c$$

where $f_c$ is the unity gain-bandwidth of the op-amp in open-loop configuration.

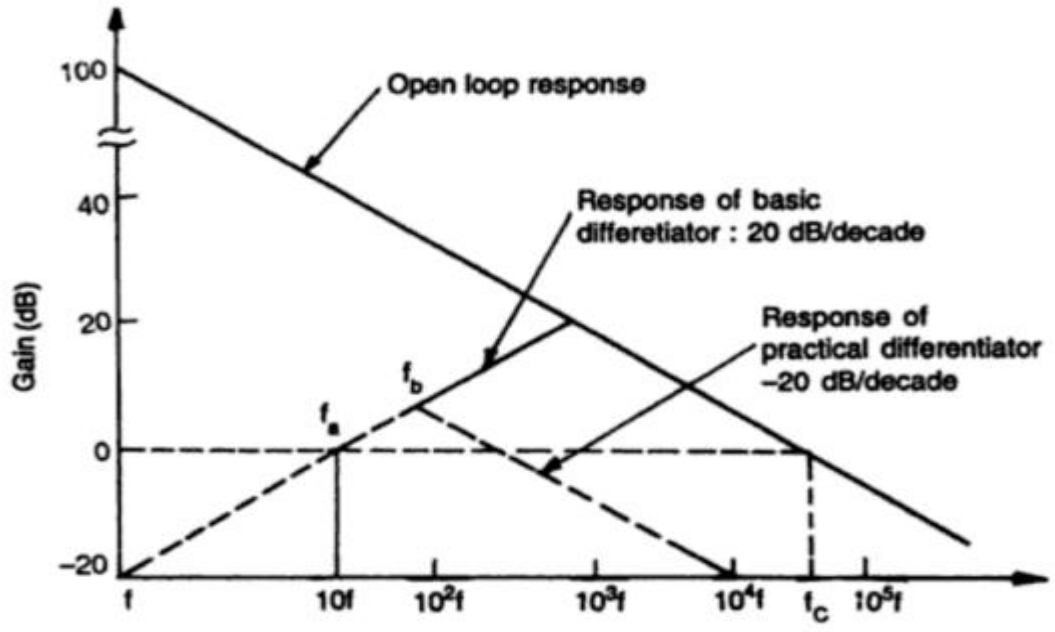


Fig. 1.3.6.2 Frequency response of Differentiator

For good differentiation, one must ensure that the time period $T$ of the input signal is larger than or equal to $R_f C_1$, that is,

$$T \geq R_f C_1$$

It may be noted that for $R_f C_1$ much greater than $R_1 C_1$ or $R_f C_f$, Eq. is reduced to, $V_o/V_i = -sR_f C_1$, that is, the expression of the output voltage remains the same as in the case of an ideal differentiator as

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

A resistance $R_{comp}$ $(= R_1 \| R_f)$ is normally connected to the (+) input terminal to compensate for the input bias circuit.

A good differentiator may be designed as per the following steps:

1. Choose $f_a$ equal to the highest frequency of the input signal. Assume a practical value of $C_1$ (< 1μF) and then calculate $R_f$.
2. Choose $f_b = 10\, f_a$ (say). Now calculate the values of $R_1$ and $C_f$ so that $R_1 C_1 = R_f C_f$.

**Example**

(a) Design an op-amp differentiator that will differentiate an input signal with $f_{max}$ = 100 Hz.
(b) Draw the output waveform for a sine wave of 1V peak at 100 Hz applied to the differentiator.
(c) Repeat part (b) for a square wave input.

(a) select, $f_a = f_{max} = 100$ Hz $= \dfrac{1}{2\pi R_f C_1}$

Let $C_1 = 0.1\ \mu F$,

then $R_f = \dfrac{1}{2\pi (10^2)(10^{-7})} = 15.9\ k\Omega$

Now choose $f_b = 10\, f_a$

$= 1$ kHz

$= \dfrac{1}{2\pi R_1 C_1}$

Therefore, $R_1 = \dfrac{1}{2\pi (10^3)(10^{-7})} = 1.59\ k\Omega$

Since $R_f C_f = R_1 C_1$,

we get, $$C_f = \frac{1.59 \times 10^3 \times 10^{-7}}{15.9 \times 10^3} = 0.01\,\mu F$$

(b) $v_i = 1 \sin 2\pi(100)t$

From Eq.

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

$$= -(15.9\ k\Omega)\ (0.1\mu F)\ \frac{d}{dt}[(1\ V) \sin (2\pi)\ (10^2)\ t]$$

$$= -(15.9\ k\Omega)\ (0.1\ \mu F)\ (2\pi)\ (10^2) \cos [(2\pi)\ (10^2)t]$$

$$= -0.999 \cos [2\pi\ (10^2)t]$$

$$= -1 \cos [(2\pi)\ (10^2)\ t]$$

The input and output waveforms are shown in Fig. (a).

(c) For a square wave input, say 1V peak and 1 KHz, the output waveform will consist of positive and negative spikes of magnitude $V_{sat}$ which is approximately 13V for ± 15V op-amp power supply. During the time periods for which input is constant at ± 1V, the differentiated output will be zero. However, when input transits between ± 1V levels, the slope of the input is infinite for an ideal square wave. The output, therefore, gets clipped to about ± 13V for a ± 15V op-amp power supply as shown in Fig. (b).

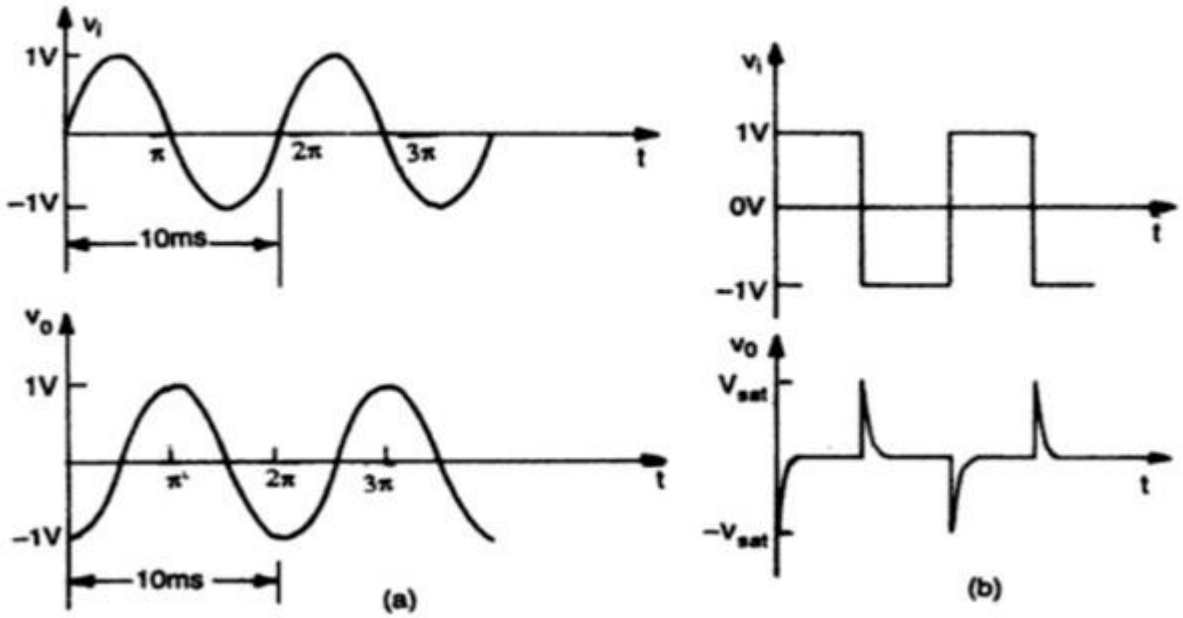


Fig. 1.3.6.3 (a) Sine-wave input and cosine output (b) Square wave input and spike output

## 1.3.7 INTEGRATOR

If we interachange the resistor and capactior of the differenetiator of Fig 1.3.6 (Differentiator), we have the circuit of Fig.1.3.7 which as we will see, is an integrator. The nodal equation at node N is,

$$\frac{v_i}{R_1} + C_f \frac{dv_o}{dt} = 0$$

$$\frac{dv_o}{dt} = -\frac{1}{R_1 C_f} v_i$$

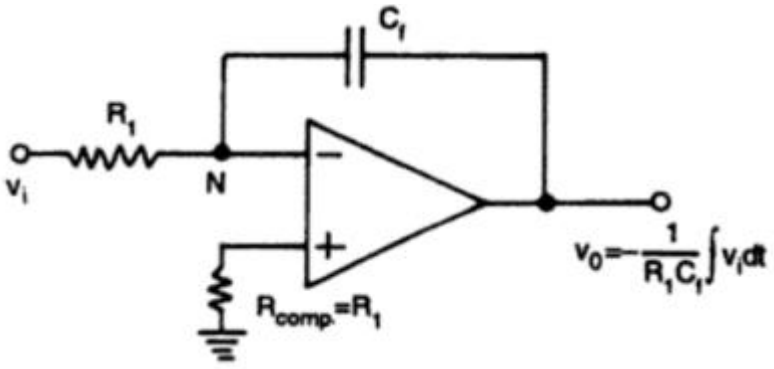


Fig. 1.3.7 Integrator

Integrating both sides, we get,

$$\int_0^t du_0 = -\frac{1}{R_1 C_f}\int_0^t v_i\,dt$$

$$v_o(t) = -\frac{1}{R_1 C_f}\int_0^t v_i(t)\,dt + v_o(0)$$

where $v_o(0)$ is the initial output voltage.

The circuit, thus provides an output voltage which is proportional to the time integral of the input and $R_1C_f$ is the time constant of the integrator. It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is also known as an inverting integrator. A resistance, $R_{comp} = R_1$ is usually connected to the (+) input terminal to minimize the effect of input bias current.

The operation of the integrator can also be studied in the frequency domain. In phasor notation, Eq. can be written as

$$V_o(s) = -\frac{1}{sR_1C_f}V_i(s)$$

In steady state, put $s = j\omega$ and we get

$$V_o(j\omega) = -\frac{1}{j\omega R_1C_f}V_i(j\omega)$$

So, the magnitude of the gain or integrator transfer function is

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1C_f}\right| = \frac{1}{\omega R_1C_f}$$

The frequency response or Bode Plot of this basic integrator is shown in the fig.1.3.7. The bode plot is a straight line of slope -6 dB/ Octave or equivalently -20 dB/Decade. The frequency $f_b$, in fig.1.3.7 is the frequency at which the gain f the integrator is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_f}$$

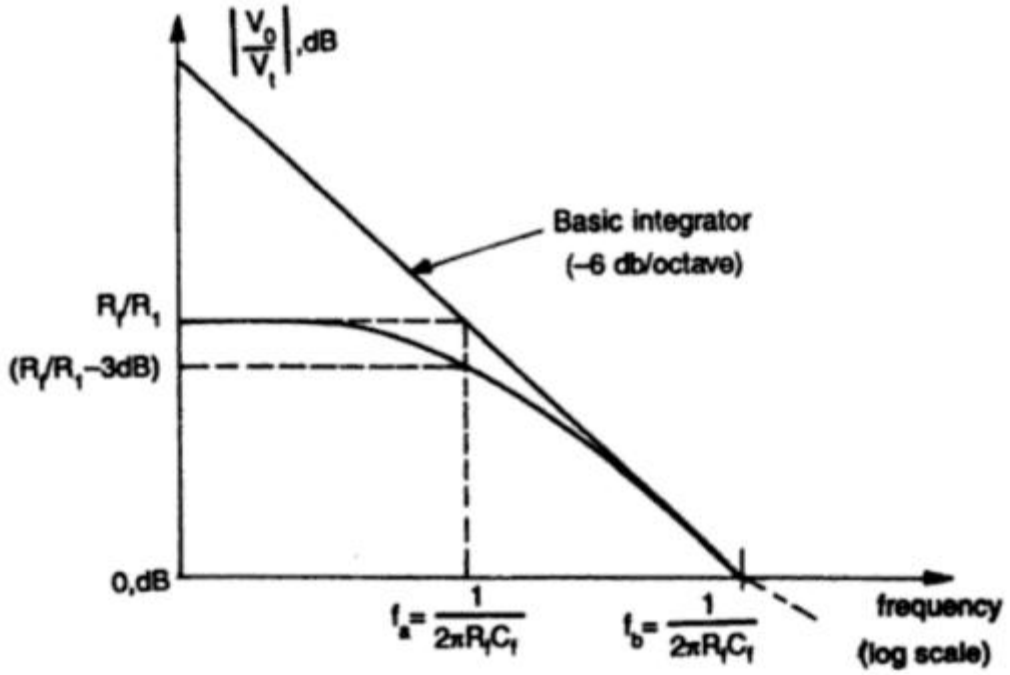


Fig. 1.3.7.1 Frequency response of basic and lossy integrator

As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc ($\omega \cong 0$), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

### 1.3.7.1 Practical Integrator (Lossy Integrator)

The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance $R_f$ as shown in Fig. 2.15 . The parallel combination of $R_f$ and $C_f$ behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called a lossy integrator. The resistor $R_f$ limits the low frequency gain to $-R_f/R_1$ (generally $R_f = 10\ R_1$) and thus provides dc stabilization.

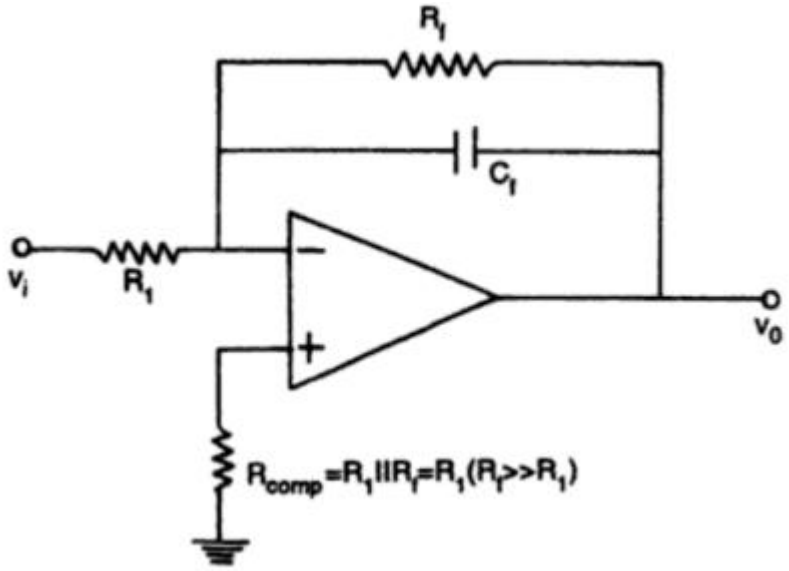


Fig. 1.3.7.2 Practical or lossy integrator

The nodal equation at the inverting input terminal of the op-amp of fig.1.3.7.1 is

$$\frac{V_i(s)}{R_1} + s C_f V_o(s) + \frac{V_o(s)}{R_f} = 0$$

from which we have,

$$V_o(s) = -\frac{1}{sR_1 C_f + R_1/R_f} V_i(s)$$

If $R_f$ is large, the lossy integrator approximates the ideal integrator. For $s = j\omega$, magnitude of the gain of lossy integrator is given by

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R_1^2 C_f^2 + R_1^2/R_f^2}} = \frac{R_f/R_1}{\sqrt{1+(\omega R_f C_f)^2}}$$

The bode plot of the lossy integrator is also shown in fig.1.3.7.1. At low frequencies gain is constant at $R_f/R_1$. The break frequency $(f=f_a)$ at which the gain is 0.707 $(R_f/R_1)$ or -3dB below its value of $R_f/R_1$ ) is claculated from Equation below

$$\sqrt{1+(\omega R_f C_f)^2} = \sqrt{2}$$

Solving for $f = f_a$, we get

$$f_a = \frac{1}{2\pi R_f C_f}$$

This is a very important frequency. It tells us where the useful integration range starts. If the input frequency is lower than $f_a$ the circuit acts like a simple inverting amplifier and no integration results. At input frequency equal to $f_a$, 50% accuracy results. The practical thumb rule is that if the input frequency is 10 times $f_a$, than 99% accuracy can result.

### 1.3.7.2 Input and output waveforms

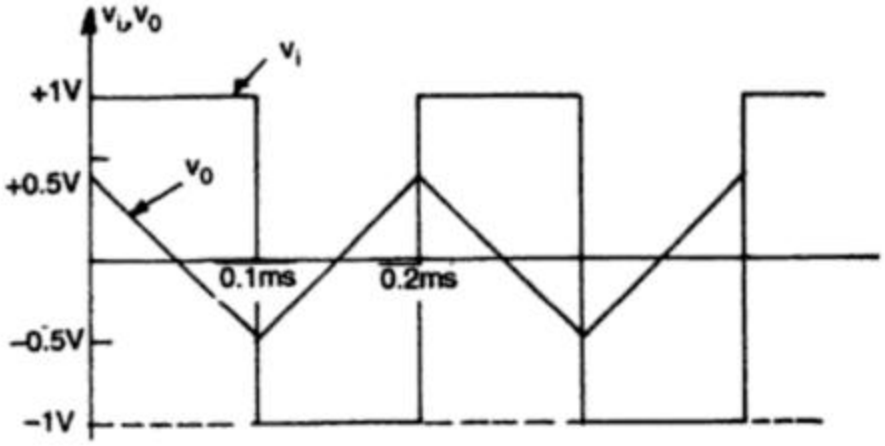


Fig. 1.3.7.3 Input and output waveforms integrator

## 1.3.8 LOGARITHMIC (LOG) AMPLIFIERS

Log-amp can also be used to compress the dynamic range of a signal. The fundamental log-amp circuit is shown in Fig. 1.3.8 where a grounded base transistor is placed in the feedback path.

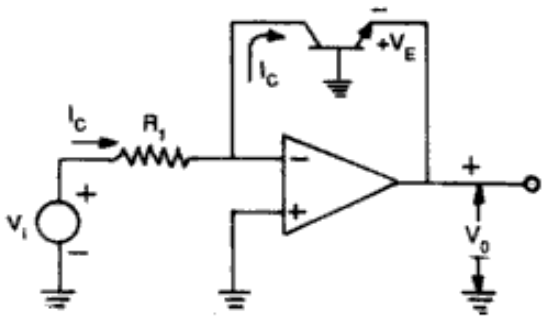


Fig. 1.3.8 Log amplifier

Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by

$$I_E = I_s \left(e^{qV_E/kT} - 1\right)$$

Since, $I_C=I_E$ for a grounded base transistor

$$I_C = I_s\,(e^{qV_E/kT} - 1)$$

$I_s$ = emitter saturation current – $10^{-13}$ A

$k$ = Boltzmann's Constant

$T$ = absolute temperature (in $^0$K)

Therefore,

$$\frac{I_C}{I_s} = (e^{qV_E/kT} - 1)$$

$$e^{qV_E/kT} = \frac{I_C}{I_s} + 1$$

$$= \frac{I_C}{I_s} \qquad [\text{as } I_s = 10^{-13}\text{ A},\ I_C >> I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right)$$

Also in Fig. 1.3.8,

$$I_C = \frac{V_i}{R_1}$$

$$V_E = -V_o$$

$$V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

$$V_{ref} = R_1 I_s$$

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find $\log_{10}$ by proper scaling

$$\log_{10} X = 0.4343 \ln X$$

The circuit however has one problem. The emitter saturation current $I_s$, varies from transistor to transistor and with temperature. Thus a stable reference voltage $V_{ref}$ cannot be obtained. This is eliminated by the circuit given in Fig. 1.3.8.1. The input is applied to one log-amp, while a reference voltage is applied to another log.amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

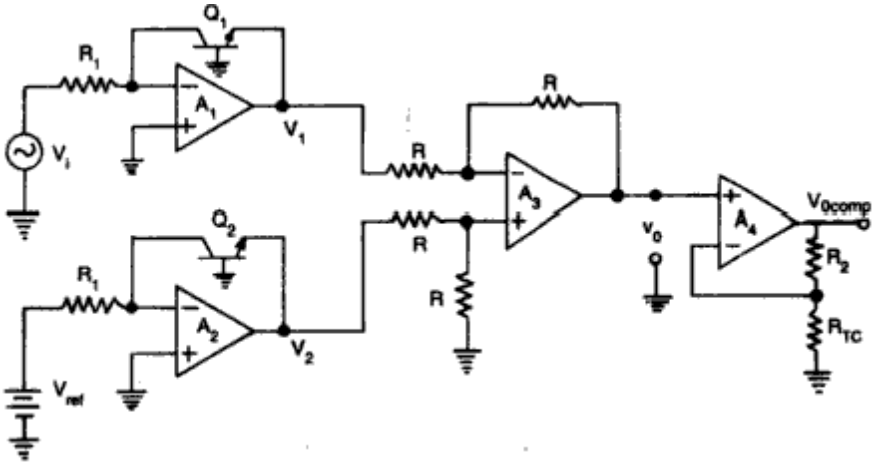


Fig.1.3.8.1. Log-amp with saturation current and temperature compensation

Assume,

$$I_{s1} = I_{s2} = I_s$$

$$V_1 = -\frac{kT}{q}\ln\left(\frac{V_i}{R_1 I_s}\right)$$

$$V_2 = -\frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

$$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right]$$

$$V_o = \frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

The voltage $V_0$ is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right)$$

where $R_{TC}$ is a temperature-sensitive resistance with a positive coefficient of temperature, so that the slope of the equation becomes constant as the temperature changes.

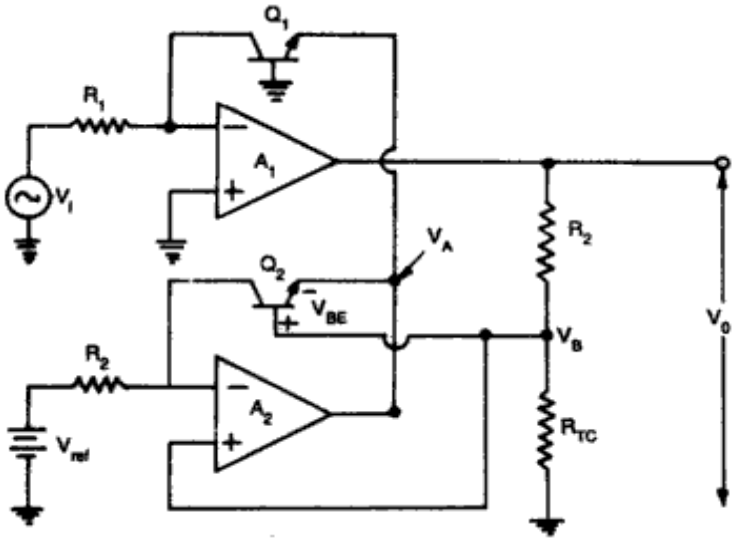


Fig. 1.3.8.2 Log-amp using two op-amps only

The circuit in Fig. 1.3.8.1 requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output can be obtained by the circuit of Fig. 1.3.8.2 using two op-amps only.

## 1.3.9 ANTILOG AMPLIFIER

The circuit is shown in Fig. 1.3.9. The input $V_i$ for the antilog-amp is fed into the temperature compensating voltage divider $R_2$ and $R_{TC}$ and then to the base of $Q_2$. The output $V_o$ of the antilog-amp is fed back to the inverting input of $A_1$ through the resistor $R_1$. The base to emitter voltage of transistors $Q_1$ and $Q_2$ can be written as

$$V_{Q1\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

$$V_{Q2\ B\text{–}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

Since the base of $Q_1$ is tied to ground, we get

$$V_A = -V_{Q1\ B\text{–}E} = -\frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right)$$

The base voltage $V_B$ of $Q_2$ is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i$$

The voltage at the emitter of $Q_2$ is

$$V_{Q2\ E} = V_B + V_{Q2\ E\text{-}B}$$

$$V_{Q2\ E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right)$$

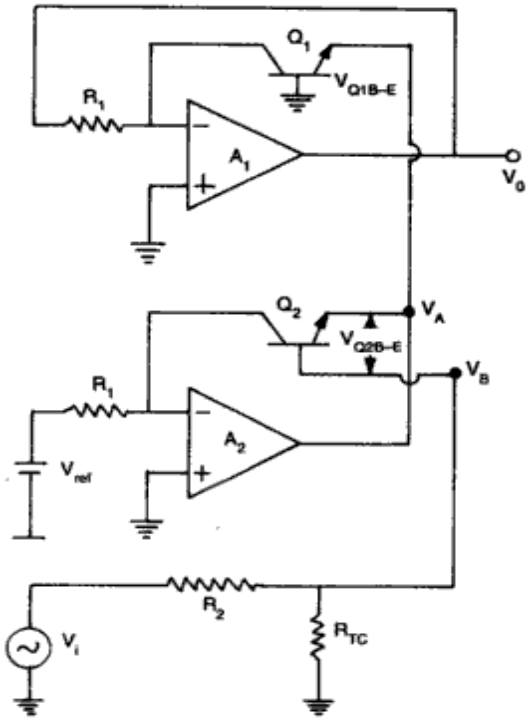


Fig. 1.3.9 Antilog amplifier

But the emitter voltage of $Q_2$ is $V_A$, that is

$$V_A = V_{Q2\ E}$$

$$-\frac{kT}{q} \ln \frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_s}$$

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q}\left(\ln \frac{V_o}{R_1 I_s} - \ln \frac{V_{ref}}{R_1 I_s}\right)$$

$$-\frac{q}{kT} \frac{R_{TC}}{R_2 + R_{TC}} V_i = \ln\left(\frac{V_o}{V_{ref}}\right)$$

Changing natural log, i.e., in to $\log_{10}$, we get

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right)$$

$$-K' V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

$$\frac{V_o}{V_{ref}} = 10^{-K' V_i}$$

$$V_o = V_{ref}\,(10^{-K' V_i})$$

Where $K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)$

Hence an increase of input by one volt causes the output to decrease by a decade. The IC755 log/antilog amplifier IC chip is available as a functional module which may require some external components also to be connected to it.

## 1.4 OP-AMP USED AS COMPARATORS

### 1.4.1 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output $\pm V_{sat}$ $(=V_{cc})$ as shown in the ideal transfer characteristics of Fig. 1.4.1(a). However, a commercial op-amp has the transfer characteristics of Fig. 1.4.1(b).

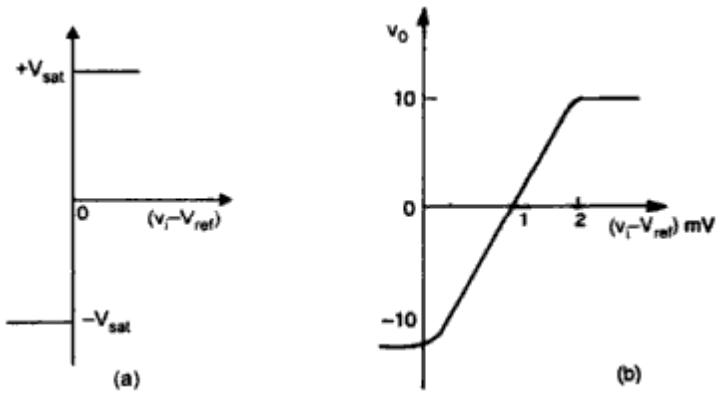


**Fig. 1.4.1 The transfer characteristics (a) ideal comparator. (b) Practical comparator**

There are basically two types of comparators:

Non-inverting comparator

Inverting comparator

The circuit of Fig. 1.4.1.1(a) is called a non-inverting comparator. A fixed reference voltage $V_{ref}$ applied to (-) input and a time varying signal $V_i$ is applied to (+) input. The output voltage is at $-V_{sat}$ for $V_i<V_{ref}$ and $V_o$ goes to $+V_{sat}$ for $V_i>V_{ref}$. The output waveform for a Sinusoidal input signal applied to the (+) input is shown in Fig. 1.4.1.1 (b and c) for positive and negative $V_{ref}$ respectively.

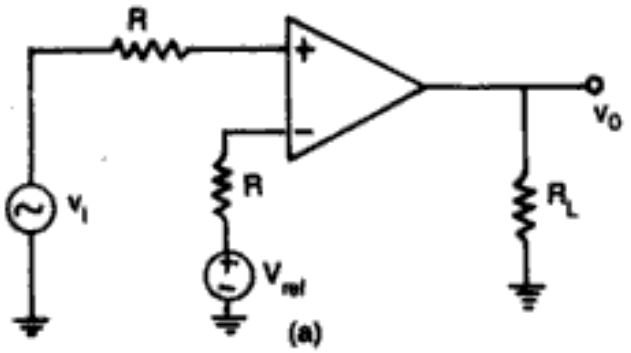


Fig. 1.4.1.1(a) Comparator

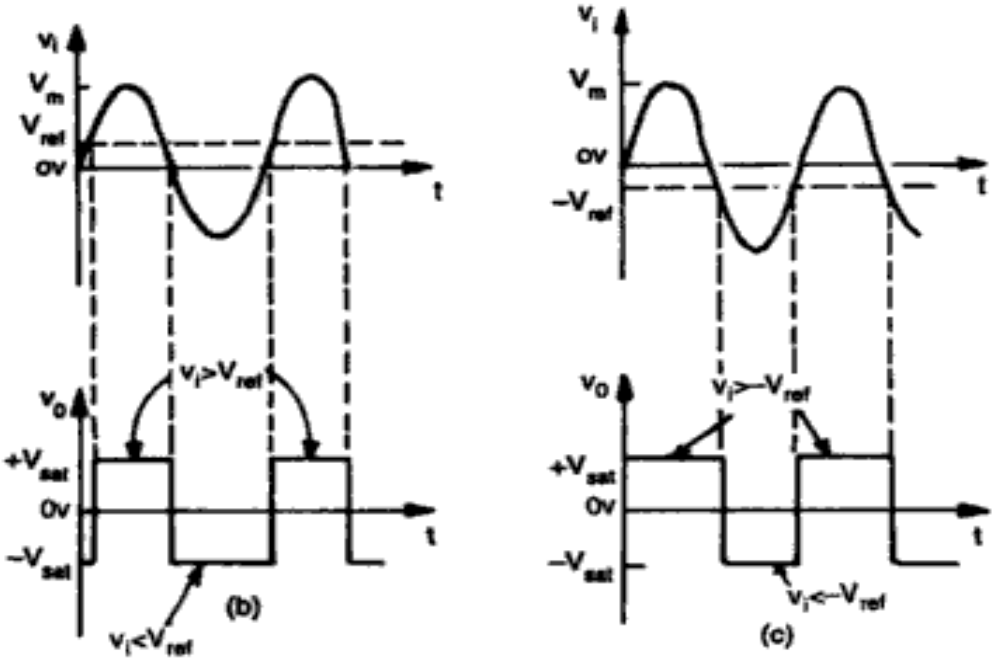


Fig. 1.4.1.1. Input and output of a Comparator when (a)$V_{ref}$>0 V (b) $V_{ref}$< 0V

In a practical circuit $V_{ref}$ is obtained by using a 10KΩ potentiometer which forms a voltage divider with the supply voltages V+ and V- with the wiper connected to (-) input terminal as shown in Fig. 1.7.4.1 (d).Thus a $V_{ref}$ of desired amplitude and polarity can be obtained by simply adjusting the 10KΩ potentiometer.

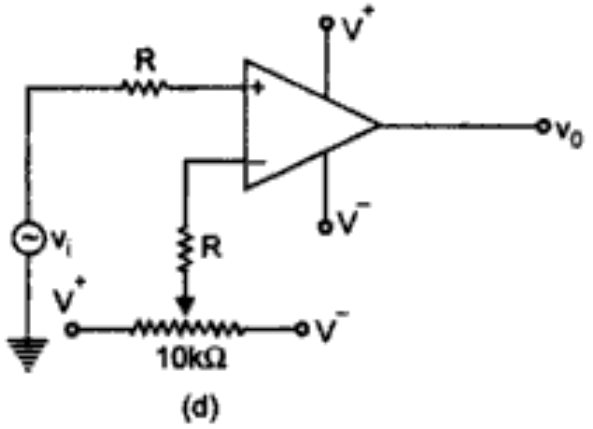


Fig. 1.7.1.1 (d) Non-inverting comparator. Input and output waveforms for (b) $V_{ref}$

Positive (c) $V_{ref}$ negative (d) Practical non-inverting comparator

Figure 1.7.1.2(a) shows a practical inverting comparator in which the reference voltage $V_{ref}$ is applied to the (+) input and $v_i$ is applied to (-) input. For a sinusoidal input signal, the output waveform is shown in Fig. 1.7.1.2(b) and (c) for $V_{ref}$ positive and negative respectively.

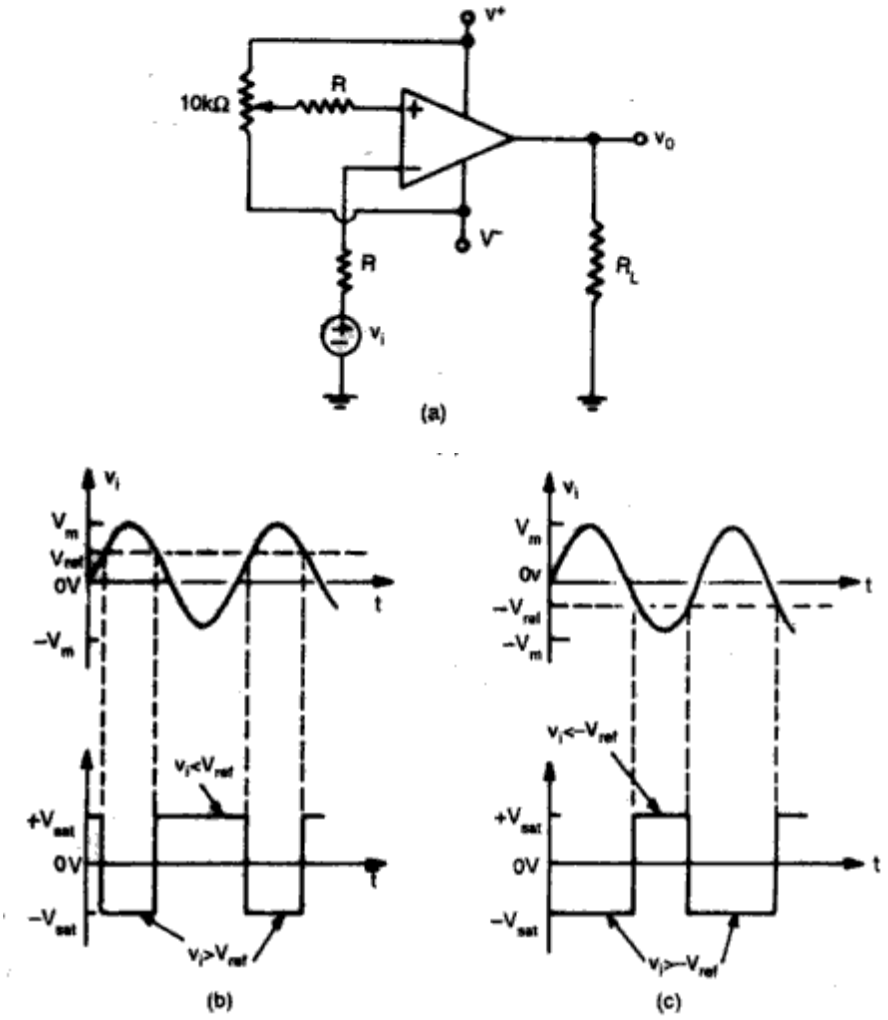


Fig. 1.7.1.2.(a) Inverting comparator. Input and output waveforms for (b) $V_{ref}$ Positive (c) $V_{ref}$ negative

## 1.7.2 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

We have seen that in a basic comparator, a feedback is not used the op-amp is used in the open loop mode. As open loop gain of op-amp is very large, very small noise voltages also can cause triggering of the comparator, to change its state. Such a false triggering may cause lot of problems in the applications of comparator as zero-crossing detector. This may give a wrong indication of zero-crossing due to zero-crossing of noise voltage rather than zero crossing of input wanted signals. Such unwanted noise causes the output to jump between high and low

states. The comparator circuit used to avoid such unwanted triggering is called *regenerative comparator or Schmitt trigger*, which basically uses a positive feedback.

The figure 1.4.2 shows the basic Schmitt trigger circuit. As the input is applied to the inverting terminal, it is also called inverting Schmitt trigger circuit. The inverting mode produces opposite polarity output. This is fed-back to the non-inverting input which is of same polarity as that of the output. This ensures a positive feedback.

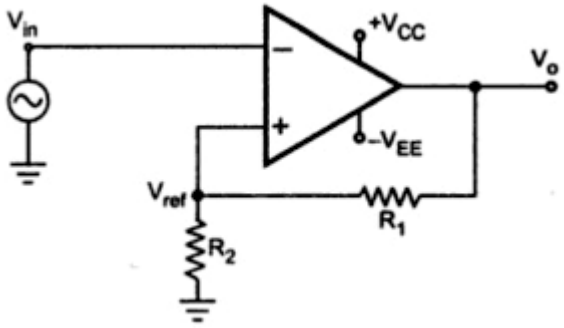


**Figure 1.4.2 Schmitt trigger using op amp.(Inverting)**

The fig.1.4.2 shows the basic inverting Schmitt trigger circuit.

- As the input is applied to the inverting terminal, it is also called inverting Schmitt trigger circuit.
- The inverting mode produces opposite polarity output (180° phase shift)
- This is fed-back to the non-inverting input which is of same polarity as that of output.
- This ensures positive feedback.

  Case 1: When $V_{in}$ is slightly positive than $V_{ref}$, the output is driven into negative saturation at $-V_{sat}$ level.

  Case 2: When $V_{in}$ is slightly negative than $V_{ref}$, the output is driven into positive saturation at $+V_{sat}$ level.

  Thus the output voltage is always at $+V_{sat}$ or $-V_{sat}$ but the voltage at which it changes its state now can be controlled by the resistance $R_1$ and $R_2$. Thus $V_{ref}$ can be obtained as per requirement.

  Now $R_1$ and $R_2$ forms a potential divider and we can write,

  *Positive saturation*

$$+V_{ref} = \frac{V_0}{R_1 + R_2} \times R_2 = \frac{+V_{sat}}{R_1 + R_2} \times R_2$$

  *Negative saturation*

$$-V_{ref} = \frac{V_0}{R_1 + R_2} \times R_2 = \frac{-V_{sat}}{R_1 + R_2} \times R_2$$

  $+V_{ref}$ is for positive saturation when $V_0 = +V_{sat}$ and is called as **upper threshold voltage** denoted as $V_{UT}$

  $-V_{ref}$ is for positive saturation when $V_0 = -V_{sat}$ and is called as **lower threshold voltage** denoted as $V_{LT}$

The values of these voltages can be determined and adjusted by selecting proper values of $R_1$ and $R_2$.

Thus

$$-V_{UT} = \frac{+V_{sat}\, R_2}{R_1 + R_2}$$

and

$$-V_{LT} = \frac{-V_{sat}\, R_2}{R_1 + R_2}$$

The output voltage remaains in a given state until the input voltage exceed the threshold volage level either postive or negative.

The fig.1.4.2.1 shows the graph of output voltage against input voltage. This is called transfer characteristics of Schmitt trigger.

The graph indicated that once the output changes its state it remains there indefinitely until the input voltage crosses any of the threshold voltage levels. This is called **hysteresis of Schmitt trigger**. The hysteresis is also called as **dead-zone** or **dead-band**.

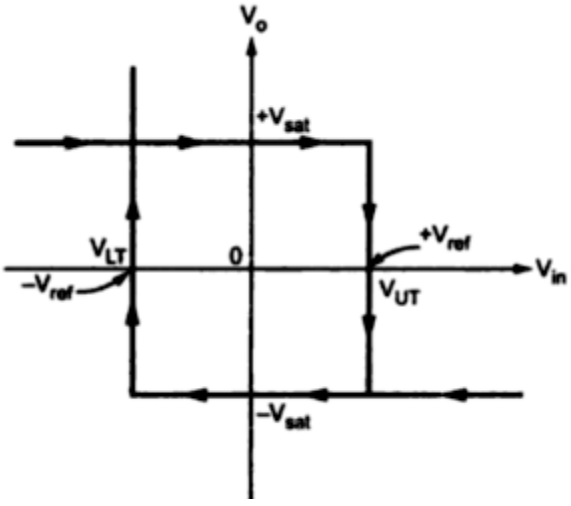


Fig. 1.4.2.1 Hysteresis of Schmitt trigger.

The difference between $V_{UT}$ and $V_{LT}$ is called width of the hysteresis denoted as H.

$$H = V_{UT} - V_{LT}$$

$$H = \frac{+V_{sat}\, R_2}{R_1 + R_2} - \frac{-V_{sat}\, R_2}{R_1 + R_2}$$

$$H = \frac{2V_{sat}\, R_2}{R_1 + R_2}$$

The schmitt trigger eliminates the effect of noise voltages less than the hysterisis H, cannot cause triggering. As for postive $V_{in}$ greater than $V_{UT}$, the output becomes $-V_{sat}$ and for negative $V_{in}$ less than $V_{LT}$, the output becomes $+V_{sat}$, this is called *inverting schmitt trigger*.

In short,

$$V_{in} < V_{LT},\ V_o = +V_{sat}$$

$$V_{in} > V_{UT},\ V_o = -V_{sat}$$

$$V_{LT} < V_{in} < V_{UT},\ V_o = Previous\ state\ achieved$$

If input applied is purely sinusoidal, the input and output waveforms for inverting Schmitt trigger can be shown as in fig.1.4.2.2.

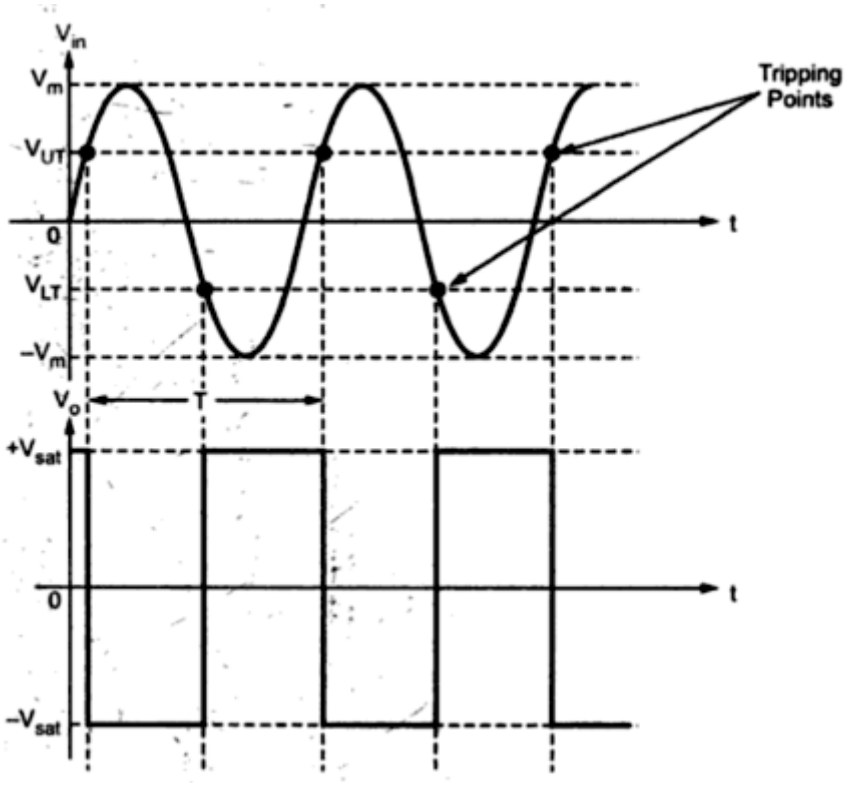


Fig. 1.4.2.2 Input and output waveforms of Schmitt trigger